

AD-A150 004

FACTORS AFFECTING SOS (SILICON-ON-SAPPHIRE) YIELD AND
RELIABILITY. (U) WESTINGHOUSE RESEARCH AND DEVELOPMENT
CENTER PITTSBURGH PA P G MCMULLIN JUL 84

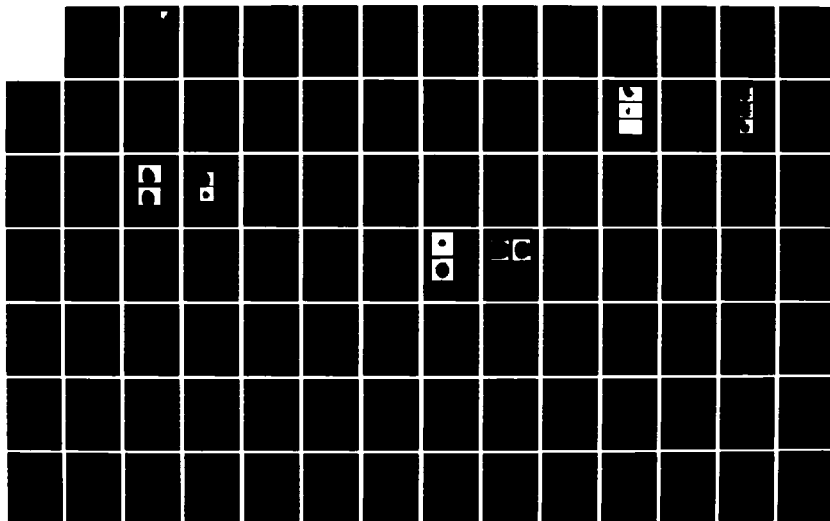
1/2

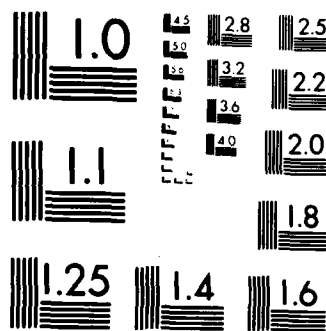
UNCLASSIFIED

83-6F4-FACTR-R1 RADC-TR-84-115

F/G 9/1

NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

12

AD-A150 004

RADC-TR-84-115

Final Technical Report

July 1984



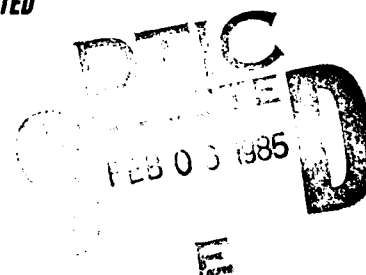
FACTORS AFFECTING SOS YIELD AND RELIABILITY

Westinghouse Electric Corporation

Dr. Paul G. McMullin

DTIC FILE COPY

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED



**ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441**

85 01 28 109

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-84-115 has been reviewed and is approved for publication.

APPROVED:

Clyde H. Lane

CLYDE H. LANE
Project Engineer

APPROVED:

John J. Bart

JOHN J. BART, Acting Technical Director
Reliability & Compatibility Division

FOR THE COMMANDER:

John A. Ritz

JOHN A. RITZ
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (RBRP) Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document requires that it be returned.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED			1b. RESTRICTIVE MARKINGS		
2a. SECURITY CLASSIFICATION AUTHORITY N/A			3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited.		
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A					
4. PERFORMING ORGANIZATION REPORT NUMBER(S) 83-6F4-FACTR-R1			5. MONITORING ORGANIZATION REPORT NUMBER(S) RADC-TR-84-115		
6a. NAME OF PERFORMING ORGANIZATION Westinghouse Electric Corp		6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Rome Air Development Center (RBRP)		
6c. ADDRESS (City, State and ZIP Code) Research & Development Center 1310 Beulah Road Pittsburgh PA 15235			7b. ADDRESS (City, State and ZIP Code) Griffiss AFB NY 13441		
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Rome Air Development Center		8b. OFFICE SYMBOL (If applicable) RBRP	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F30602-81-C-0146		
8c. ADDRESS (City, State and ZIP Code) Griffiss AFB NY 13441			10. SOURCE OF FUNDING NOS.		
			PROGRAM ELEMENT NO. 62702F	PROJECT NO. 2338	TASK NO. 01
			WORK UNIT NO. 1J		
11. TITLE (Include Security Classification) FACTORS AFFECTING SOS YIELD AND RELIABILITY					
12. PERSONAL AUTHOR(S) Dr. Paul G. McMullin					
13a. TYPE OF REPORT Final		13b. TIME COVERED FROM 15 Apr 81 to 15 Apr 83		14. DATE OF REPORT (Yr., Mo., Day) July 1984	
				15. PAGE COUNT 188	
16. SUPPLEMENTARY NOTATION N/A					
17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)		
FIELD	GROUP	SUB. GR.			
09	01		Silicon-On-Sapphire, Integrated Circuits, Scattering		
11	06		SOS Characterization, Haze, XTEM		
			Yield, Stress		
19. ABSTRACT (Continue on reverse if necessary and identify by block number) This report describes methods for characterizing the quality of silicon-on-sapphire (SOS) wafers to improve the yield and reliability of integrated circuits fabricated in this material. Epilayer stress was measured by Raman lineshift. Epilayer surface haze was quantitatively measured by ultraviolet scattering. Epilayer defect densities were studied by XTEM. MOSFET transistors were fabricated in characterized wafers and electrically tested to determine yield. Device yields were very low in very high haze wafers with epilayers deliberately grown at suboptimal temperatures. There is no statistically significant correlation between haze or layer stress and yield for vendor wafers or for epilayers grown at nominally optimal temperatures.					
20. DISTRIBUTION/AVAILABILITY OF ABSTRACT UNCLASSIFIED/UNLIMITED <input type="checkbox"/> SAME AS RPT <input checked="" type="checkbox"/> DTIC USERS <input type="checkbox"/>			21. ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED		
22a. NAME OF RESPONSIBLE INDIVIDUAL Clyde H. Lane			22b. TELEPHONE NUMBER (Include Area Code) (315) 330-3473		22c. OFFICE SYMBOL RADC (RBRP)

DD FORM 1473, 83 APR

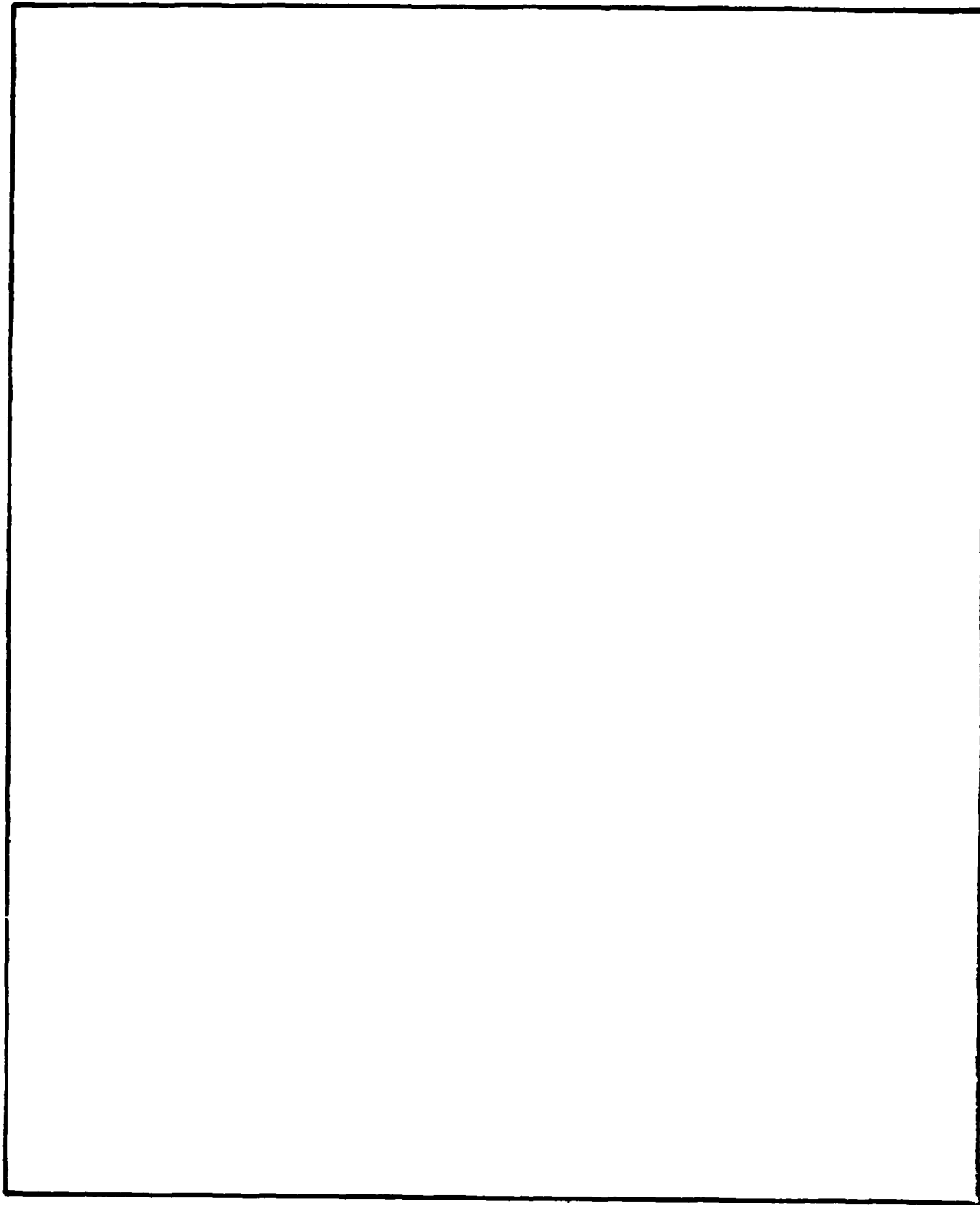
EDITION OF 1 JAN 73 IS OBSOLETE.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE



UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

TABLE OF CONTENTS

LIST OF FIGURES.....	iii
LIST OF TABLES.....	ix
1. INTRODUCTION.....	1
1.1 Review of SOS Characterization Methods.....	1
1.2 Methods Selected for Study.....	3
1.3 SOS Wafers Obtained for Study.....	5
2. CHARACTERIZATION BY STANDARD METHODS.....	8
2.1 Wafer Flatness.....	8
2.2 Wafer Bow.....	11
2.3 Epilayer Thickness Measurements.....	15
2.4 X-ray Orientation and Rutherford Backscattering....	28
2.4.1 Rutherford Backscattering Measurements.....	37
3. CHARACTERIZATION BY NEW METHODS.....	45
3.1 Raman Spectroscopic Measurement of Layer Stress....	45
3.1.1 Raman Method.....	47
3.1.2 Raman Layer Stress Data.....	52
3.2 Ultraviolet Scattering Haze Measurement.....	60
3.2.1 Introduction.....	60
3.2.2 Ultraviolet Scattering Method.....	61
3.2.3 UVS Haze: Scattering Angle Scans.....	65
3.2.4 UVS Haze Measurements.....	69
3.2.4.1 UVS Haze Method.....	69
3.2.4.2 UVS Qualification Data.....	70
3.2.4.3 UVS Haze Measurement Data.....	73
3.2.4.4 Comparison of UVS and UVR Haze Measurements.....	78
3.2.5 UVS Rotation Angle Scans.....	82
3.2.6 Sources of UVS Haze.....	95

4. ADDITIONAL CHARACTERIZATION.....	106
4.1 Cross-Section Transmission Electron Microscopy (XTEM).....	106
4.1.1 XTEM Technique.....	106
4.1.1.1 TEM Defect Analysis of Microtwins in SOS.....	107
4.1.2 XTEM Results.....	113
4.2 Current DLTS Measurements on SOS Transistors.....	121
5. DEVICE FABRICATION AND TESTING.....	134
5.1 Fabrication Procedure.....	134
5.2 Test Method and Data Tabulation.....	138
6. STATISTICAL ANALYSIS.....	147
6.1 Device Fabrication and Electrical Testing.....	147
6.2 Statistical Analysis of Test Data.....	152
7. DISCUSSION OF RESULTS AND CONCLUSIONS.....	164
8. REFERENCES.....	169

Accession For	
NTIS GRA&I	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By	
Distribution/	
All Security Codes	
Distribution, or	
Distribution	
A-1	



LIST OF FIGURES

Figure 1.	SOS wafer flatness measurement under a) 5 inches of vacuum, b) 25 inches of vacuum, c) calibration wedge.	10
Figure 2.	Wafer flatness interferograms -- 0.67 microns per fringe: a) very flat wafer, b) "roof-shaped" wafer, c) tapered wafer.	12
Figure 3.	Distribution of wafer flatness data from interferograms.	13
Figure 4.	Interferograms showing the unconstrained shapes of wafers W37F and W41F; the calibration is 4.75 $\mu\text{m}/\text{fringe}$.	16
Figure 5.	Wafer bow interferograms -- 4.8 microns/fringe): a) least bowed, b) most bowed.	17
Figure 6.	Distribution of wafer bow data from interferograms.	18
Figure 7.	Initial reflectivity data for selected vendor wafers showing measurement locations and orientation of etched stripes.	21
Figure 8.	Talystep surface profile of measurement point on W58F; height of step indicates thickness of epilayer.	23
Figure 9.	Epilayer thickness versus position along etched stripe in wafers W32F and W58F.	24
Figure 10.	Distribution of average layer thickness.	27
Figure 11.	Distribution of vendor data on layer thickness.	28
Figure 12.	Distribution of the difference between vendor layer thickness data and Westinghouse data for 110 wafers.	30
Figure 13.	Distribution of layer thickness measurements of 550 data points on 110 wafers.	31
Figure 14.	Distribution of thickness variation.	32

Figure 15.	Distribution of the rms variation of layer thickness on single wafers.	34
Figure 16.	X-ray diffraction patterns for two SOS wafers. The relative orientations of the wafers are shown as well as the angular orientations of the peaks of optical scattering.	35
Figure 17.	X-ray diffraction pattern for W61F; the X-ray beam directions are shown in the drawing. For this Type I wafer, the c-axis is shown to lie 45° counterclockwise from the wafer flat.	36
Figure 18.	Rutherford backscattering spectrum from vendor wafer W18F.	40
Figure 19.	Rutherford backscattering spectrum from low-temperature epi wafer W312F.	43
Figure 20.	Schematic of experimental set-up for Raman scattering.	48
Figure 21.	Raman spectra of SOS and bulk silicon wafers.	50
Figure 22.	Comparison of SOS wafer and silicon standard to determine effect of narrowing the slits down on the spectral resolution.	51
Figure 23.	Distribution of Raman shift data for vendor wafers.	53
Figure 24.	Distribution of Raman data for Westinghouse wafers excluding low-temperature epi.	55
Figure 25.	Distribution of Raman data for low-temperature epi wafers.	56
Figure 26.	Raman linewidth for three groups of wafers: group 1, vendor wafers; group 2, low-temperature epi wafers; group 3, silicon wafers	57
Figure 27.	Distribution of Raman data from silicon wafers.	58
Figure 28.	Sources of haze.	59
Figure 29.	Apparatus for measurement of UV scattering haze.	63
Figure 30.	Intensity of scattered UV light versus scattering angle θ .	67

Figure 31.	Scan taken with mercury arc lamp optical source.	68
Figure 32.	Histogram of the haze numbers versus haze readings for the vendor wafers.	75
Figure 33.	Westinghouse haze readings from UV scattering plotted versus vendor haze readings from UV reflectivity for 105 vendor wafers.	81
Figure 34.	Setup for UV scattering haze angular dependence.	84
Figure 35.	UV scattering versus rotation angle for two vendor SOS wafers.	85
Figure 36.	UV scattering versus rotation angle as a function of UV wavelength for vendor wafer W78. The scan starts at 50° CCW from the zero reference angle, or nominally 90° before the first major peak.	88
Figure 37.	UV scattering versus rotation angle as a function of UV wavelength for vendor wafer W82. The scan starts at 40° , or nominally 90° before the first major peak.	89
Figure 38.	UV scattering versus rotation angle as a function of UV wavelength for Westinghouse epi wafer W401.	90
Figure 39.	UV scattering versus rotation angle for low-temperature epi wafer W309.	92
Figure 40.	UV scattering versus rotation angle for two Kyocera 4-inch SOS wafers.	93
Figure 41.	UV scattering versus rotation angle for Union Carbide 4-inch SOS wafers.	94
Figure 42.	Silicon optical data from Aspnes and Studna.	97
Figure 43.	UV scattering versus rotation angle: a) SOS wafers with bare silicon surface, b) same wafers after evaporation of 50 nm aluminum onto surface.	98
Figure 44.	UV scattering versus rotation angle: a) W93 with 50 nm of aluminum on surface, b) substrate of W93 with 100 nm of silver on surface.	99

Figure 45.	UV scattering versus rotation angle for a sample with a stripe pattern fabricated on the surface.	101
Figure 46.	Talystep traces on W98 in different directions relative to c-axis projections.	103
Figure 47.	Nomarski differential interference contrast micrographs at 2000 X.	104
Figure 48.	Schematic illustrating procedure for preparing cross-sectional TEM specimens of silicon on sapphire.	108
Figure 49.	a) Schematic showing electron diffraction pattern of a $\langle 110 \rangle$ zone in diamond-type silicon crystal. b) Same pattern as in a) showing location of (111) twinning plane and two twin spots (asterisks) formed by reflection through the twinning plane. c) Same pattern as in a) showing all possible parent crystal and twin diffraction spots; filled circles are parent crystal, open circle one set of twin reflections, X's second set of twin reflections. d) Arc of strong diffraction spots caused by tilting crystal slightly off axis; two strong twin spots are indicated.	109
Figure 50.	a) Bright field micrograph showing two sets of microtwins in SOS imaged under conditions shown in Figure 49d. b) Electron diffraction pattern showing arc of strong reflects; the two twin reflections are indicated. c) and d) Dark field micrographs individually showing each set of twins formed by using twin spots shown in d.	112
Figure 51.	XTEM view of W75F along 110 direction, showing twins on $\bar{1}11$ (majority) and $1\bar{1}1$ (minority) planes.	114
Figure 52.	Orientation of twin planes and viewing directions for XTEM views; the silicon (111) planes are shown projecting downward into the epilayer.	115
Figure 53.	Dark field XTEM views of W75F along $\bar{1}10$ direction, showing twins on $\bar{1}\bar{1}0$ (majority) and 111 (minority) planes.	117
Figure 54.	XTEM views of W96F along $\bar{1}10$ direction showing twins on $\bar{1}\bar{1}1$ (majority) and 111 (minority) planes.	118

Figure 55.	XTEM views of surface asperities where twin planes intersect surface.	120
Figure 56.	XTEM views of W88F along 100 directions showing both majority sets of twins: a) bright field view showing extended defect structures, b) and c) higher magnification views of two extended defect regions.	122
Figure 57.	Current DLTS set-up.	125
Figure 58.	Block diagram of automated current DLTS system.	126
Figure 59.	Structure of SOS MOSFET: a) top view, b) cross section. The gate length is 2 μm and width is 40 μm .	128
Figure 60.	I-V characteristics of SOS MOSFET (5425-7-7-L) used as DLTS test device: a) drain current saturated, b) drain current varying linearly with drain voltage. Current DLTS measurements are made with the MOSFET biased in the linear region, as in (b).	129
Figure 61.	Sample exhibiting peak in current DLTS measurement: SOS chip 5425-7-7, transistor L, $V_{\text{DS}} = 50.8 \text{ mV}$, $V_{\text{GS}} = 2.00 \text{ V}$.	130
Figure 62.	Sample exhibiting no peak in current DLTS measurement: SOS chip 71-5, transistor 11, $V_{\text{DS}} = 50.7 \text{ mV}$, $V_{\text{GS}} = 2.0 \text{ V}$.	133
Figure 63.	Calcomp plot of transistor array (a) and large-area capacitor (b).	135
Figure 64.	Sample I-V Curves.	139
Figure 65.	Sample printout of test data.	141
Figure 66.	Chip map.	143
Figure 67.	I-V curve showing high source-to-drain current.	144
Figure 68.	I-V curve showing damage resulting from short silicon etch.	145
Figure 69.	Device yield results for all SOS wafers fabricated.	153
Figure 70.	Device yields for vendor wafers.	156

Figure 71. Device yields for all vendor wafers, plotted against vendor-supplied UV reflectivity haze data.	157
Figure 72. Device yields for Run 1.	158
Figure 73. Device yields for Run 2.	160
Figure 74. Device yields for Run 3.	161
Figure 75. Device yields for Run 4.	162

LIST OF TABLES

Table 1.	SOS Wafer Specifications	6
Table 2.	Westinghouse Epilayers	7
Table 3.	Epilayer Thickness Data	29
Table 4.	Rutherford Backscattering Results	42
Table 5.	Summary of Raman Results for SOS Wafers	54
Table 6.	Repeatability Data with the Average Reading and rms Variation	72
Table 7.	Ultraviolet Scattering Haze Measured on 106 Vendor Wafers	74
Table 8.	Summary of UVS Haze Statistics	76
Table 9.	UVR Haze Numbers Supplied by the Vendor	80
Table 10.	Twin Densities Determined from XTEM Views	116
Table 11.	Results of Current DLTS Measurements	132
Table 12.	NMOS and PMOS Process Description	137
Table 13.	Summary of Contact Resistance Measurements	146
Table 14.	Processing Yield Analysis	148
Table 15.	Analysis of Wafers Spoiled in Processing in Runs 2-4	148
Table 16.	Summary of Electrical Test Results	151
Table 17.	Linear Correlation with Haze Number	154
Table 18.	Statistical Significance of Yield Correlations	163

1. INTRODUCTION

The objective of this program was to develop techniques for nondestructive evaluation of silicon-on-sapphire films and to relate the parameters of the starting material to the performance and yield of devices fabricated in the material.

To accomplish this objective, a large number of SOS wafers were purchased from a commercial supplier or grown under varied conditions in our laboratory. The wafers were characterized by nondestructive techniques suitable for eventual use as quality assurance screening tests. In addition, selected wafers were characterized by methods which are destructive or too costly for quality screening, but add information on the physical condition of the material. Test structures including active devices were fabricated in the SOS wafers and electrically tested to provide yield and performance data. The yield data were analyzed to identify significant factors relating starting material parameters to device yield.

1.1 Review of SOS Characterization Methods

Many techniques have been used to characterize the electrical and structural properties of SOS wafers. The electrical techniques are difficult because of the submicron thickness of the silicon epi layer. In such a thin layer, the silicon surface and the silicon sapphire interface exert a strong influence on electrical behavior. The influence of the surface can be controlled by depositing an oxide and an electrode to adjust the surface potential.⁽¹⁾ This allows determination of film resistivity by a modified Van der Pauw (MVDP) technique with the four electrical contact points located near the edge of the wafer. The MVDP method has also been applied without surface passivation.⁽²⁾

Four-point probe measurements have also been used to detect low film resistivity caused by contamination during growth.⁽²⁾ More detailed information on the effective band structure and deep levels has been obtained from surface photovoltage measurements.⁽³⁾

The structural characteristics of SOS have been established by TEM studies. Cross-sectional TEM shows the high density of microtwins that comprise the predominant crystallographic defect in the silicon epilayer.^(4,5) High-resolution TEM has established that the silicon-sapphire interface is locally free of defects.⁽⁶⁾ Defects can also be observed through Rutherford backscattering (RBS), which provides a depth profile of defect density.⁽⁷⁾

Electron beam channeling can also give a quantitative measure of crystal perfection.⁽⁸⁾ Electron channeling is a diffraction process based on the scattering of electrons from a selected crystal plane. By measurement of the scattered signal at a selected region on the Kikuchi figure, an index of crystal perfection is derived. X-ray diffraction techniques are also used for the same purpose. Rocking curves measure the FWHM of diffraction peaks analogous to the e-beam channeling.⁽⁹⁾ X-ray pole figures allow a measurement of the volume fraction of microtwins located on the four allowed twin planes.⁽¹⁰⁾ Crystal perfection can also be roughly assessed by etching techniques.⁽¹¹⁾ The composition of the silicon epilayer can be determined, within sensitivity limits, by SIMS.⁽¹²⁾

Optical techniques have been applied to evaluate SOS quality. Visual inspection and classification by judgement of surface haze has been an accepted practice for SOS wafer inspection.⁽²⁾ The surface reflectance at ultraviolet wavelengths has been shown to be related to crystal quality.⁽¹³⁾ Raman shift spectroscopy can be used to measure the compressive stress in the silicon epilayer.⁽¹⁴⁾

1.2 Methods Selected for Study

The objective of the program was to develop methods for quality assurance for as-grown SOS wafers. Optical methods were considered as being nondestructive, rapid, and inexpensive enough to allow screening of every wafer before fabrication. The visual haze inspection method that had been used in the industry is an acceptance test for SOS wafers. For this program, the primary method for characterization was designed to be a quantitative, precise equivalent to the visual haze inspection. Haze as perceived by the human eye is the result of scattering of light from the surface of the wafer at angles widely separated from the specular reflectance angle of the directly reflected light. The method of UV scattering haze measurement, described in Section 3.2.1, accurately measures the low level of ultraviolet light scattered at the silicon epilayer surface. The scattered light intensity is expected to be related to crystal quality through the causes of scattering. Light may be scattered by inhomogeneities in the material, giving a scattering signal proportional to the density of crystal defects or other nonuniformities in the epilayer. Scattering may also arise from surface facets or asperities. The surface of an SOS wafer may be indicative of the epilayer quality in a way that is not true for bulk silicon wafers. The SOS surface represents a crystal growth interface with the vapor phase source of silicon. Crystal defects in the layer can be expected to produce surface features through local disruption of the crystal growth process that would otherwise exist on a uniform crystal facet. Bulk wafers are cut and polished, so no traces exist on the surface of crystal growth processes. Although there were no prior reports to establish a definite connection between crystal defects and surface scattering, the reliability of visual haze as a quality index⁽²⁾ indicated that such a connection did exist. The UV scattering method offers some operational advantages over the UV reflectance method. For reflectance measurements, it is necessary to measure the difference between relatively large numbers; namely, the intensity of the direct reflection from an SOS wafer and the reflection

from a silicon standard. This creates the usual difficulty in maintaining high accuracy of the directly measured quantities so that the difference will be precise. For scattering measurements, a very small quantity is measured directly. The scattered light signal is many orders of magnitude smaller than the directly reflected light signal, but the highly sensitive photomultiplier tube detector allows very precise measurements. This comparison is explained further in Section 3.

The measurement of epilayer stress by Raman scattering spectroscopy was also selected as a primary characterization method. The physical basis of Raman shift measurements of stress had been established for silicon bulk samples and for SOS wafers. However, there was no information about the variations in stress that might be observed in wafers from production runs, or among wafers grown under different conditions. Since the layer stress in itself is a major factor affecting electron mobility, an effort was planned to determine whether stress could be a yield factor as well. The Raman peak linewidth was also to be investigated as an indicator of local stress nonuniformity.

Standard methods of optical interferometry were used to measure wafer bow and flatness, and epilayer thickness was measured by reflectance interferometry. The substrate orientation was checked by X-ray. The purpose of standard measurements was to determine how well the vendor wafers met the specifications and to identify any problems in wafer conformation. More detailed techniques were used to assess the defect structure of selected wafers. Rutherford backscattering was used to verify that low-temperature epilayers were of lower quality as intended. Cross-section TEM micrographs were used to determine microtwin densities on the major and minor twin planes for comparison with haze measurements. When the rotation angle dependence of UV scattering was discovered, additional surface texture characterizations by Nomarski differential-interference contrast optical microscopy and by profilometry were performed. Conductivity DLTS measurements were made

on the fabricated devices to observe trap levels that might arise from contamination during processing.

1.3 SOS Wafers Obtained for Study

A total of 110 SOS wafers were purchased for this program from Union Carbide, Crystal Products Division. The specifications were consistent with the then current requirements of Westinghouse ATL in order to be sure that these wafers would be processed in the same way as their SOS products. The specifications were typical for industry orders of the time. The 2-inch wafers were to have a 500 nm thick epilayer with a 10% tolerance. Substrate orientation, wafer dimensions, and visible defects were also specified, as shown in Table 1.

For identification purposes, each vendor wafer was assigned a number, from W1F to W110F, in sequence. The prefix W and suffix F serve to identify the wafers as part of this program and are sometimes omitted. Most of the wafers have their number scribed into the epilayer near the rim diametrically opposite the flat.

In addition to the SOS wafers, 55 sapphire substrates were purchased from the vendor, Union Carbide. The specifications were the same as for the SOS substrates. These substrates were used for epilayer growth at Westinghouse to study the effects of varying growth conditions on the characterization methods and on device yield. Some 2-inch substrates were also obtained from Kyocera under another program and exchanged for some of our Union Carbide substrates.

The silicon epilayers were deposited in a horizontal reactor with hydrogen carrier gas and silane source gas. The graphite susceptor was coated with silicon carbide before epi runs to prevent contamination. The principal variable of the epi runs was the deposition temperature. Runs at 880 and 900°C (optical pyrometer uncorrected) were intended to have suboptimal epilayer quality. Runs at 970 and 1000°C were close to the optimum for our system as determined in separate experiments. A summary of the Westinghouse epi runs is shown in Table 2.

Table 1
SOS Wafer Specifications

Substrate:

1. Crystalline Sapphire: (Al_2O_3), no slip, twins, or lineage
2. Orientation: $1\bar{1}02 \pm 2^\circ$
3. Diameter: $2.000 \pm .010$ inches
4. Thickness: $.013 \pm .002$ inches
5. Flat Location: parallel to (110) silicon plane and $0\bar{1}21$ sapphire plane $\pm 20^\circ$
6. Flat Width: $.675 \pm .125$ inch
7. Out of Roundness: .050 maximum
8. Bow: 250 μm maximum
9. Taper: 50 μm maximum
10. Finish: front - epi polish
back - fine ground
11. Pits: no more than 4 pits/substrate; less than 50 μm diam.
12. Scratches: none longer than 0.5 inches
90 of 100 wafers to have no scratches
13. Cracks: none
14. Edge Chips: less than 10/substrate; no chips more than .040 inches deep
15. Material: new material only; no repolished wafers

Epilayer:

1. Dopant: intrinsic
2. Resistivity: greater than 50 ohm-cm
3. Thickness: $0.5 \mu\text{m} \pm 10$ percent
4. Surface Finish: no visible spikes
5. Orange peel: none
6. Haze: no visible haze

Table 2
Westinghouse Epilayers

Number of Wafers	Wafer Number	Deposition Temperature	Substrate
6	301-306	880	Union Carbide
6	307-312	900	Union Carbide
6	401-406	1000	Union Carbide
4	407-410	1000	Kyocera
6	411-416	970	Kyocera
4	417-420	970	Union Carbide
4	421-424	900	Union Carbide

The wafer numbers run in the 300-400 range to distinguish them from the vendor SOS wafers. Elsewhere in the report these wafer numbers appear with the W-F prefix-suffix notation.

Additional wafers were available at various times during the program and were characterized by some of our techniques. Several wafers fabricated by the solid-phase epitaxial regrowth method, under a separate contract (VHSIC Phase III Improved SOS, Contract No. F33615-79-C-1946, Wright-Patterson), were characterized for layer stress by Raman spectroscopy. Recently, sample lots of 4-inch SOS wafers from Union Carbide and Kyocera were acquired by Westinghouse ATL Division for evaluation. These were characterized for UVS haze and rotation angle dependence of haze. Results of the characterizations are reported in the appropriate sections.

2. CHARACTERIZATION BY STANDARD METHODS

2.1 Wafer Flatness

The wafer flatness is measured as the deviation from flatness of the epilayer surface when the back surface of the wafer is held by vacuum against a flat reference surface. This measurement therefore indicates the thickness uniformity of the wafer. This parameter is of critical importance for photolithography processes during device fabrication. If the wafer is not flat, it will not be possible to get a good focus over the whole wafer for a projection mask. Regions which are out of focus will not be properly registered and exposed, decreasing the device yield in such areas. Wafer flatness becomes even more important when device dimensions are scaled downward, closer to optical wavelengths. By using shorter wavelength light and diffraction-limited lenses to get barrier resolution, the depth of focus is decreased and wafer flatness specifications must be tightened.

Two special considerations must be taken into account in specifying wafer flatness. First, it can be seen that a simple taper of wafer thickness will not prevent proper focussing; that is, if the wafer thickness varies linearly with the position. Secondly, it is now a common practice to expose one chip at a time on the entire wafer by direct-step-on wafer (DSW) photolithography. For correct DSW focussing, flatness must be maintained only in the area exposed, which is typically smaller than 1 cm^2 . The appropriate specification for DSW processing is expressed as a deviation from flatness within an exposure range, for example, 2 microns per inch. Finally, it can be mentioned that other pattern deposition techniques, such as X-ray and electron beam lithography, have greater depth of field and are less sensitive to wafer flatness.

The wafer flatness measurements were made on a Tropel model 9000 wafer flatness analyzer, an optical interferometric instrument of adjustable sensitivity. Wafers were mounted on a 2-inch diameter Perkin-Elmer type vacuum chuck, identical to vacuum fixtures typically used for photolithography. The wafer and vacuum fixture were dusted by dry nitrogen passed through a 3M brand static eliminator to remove all dust.

The entire surface of the wafer is shown in contour map form as seen in Figures 1a and b. Each dark fringe in the pattern represents a contour of constant thickness. The surface of the vacuum chuck is also visible in the figure, and adjustments on the Tropel instrument have been used to level the chuck within one fringe of tilt. The backside of the wafer is thus held by vacuum against a flat, level surface. The interval between fringes is adjustable by an instrument setting. Figure 1c shows the calibration of the given setting by an optical wedge of known taper. There are 22 fringes in the 20.2 μm taper of the wedge, yielding a calibration of 0.92 μm per fringe.

High and low areas on the wafer are identified by applying light pressure to the fixture which holds the vacuum chuck. The fringes move away from high points and toward low areas. The highest point on the test wafer in Figure 1 is the circular fringe near the center, and the lowest point is at the rim near the 10 o'clock position. There are 9.5 fringes between high and low points, or 8.7 μm , when the vacuum applied is 5 inches. At 25 inches of vacuum, the wafer changes shape slightly so there is about 9.7 μm of thickness variation. This probably indicates that at the lower vacuum, the wafer backside was not in conformity with the surface of the chuck. Measurements for this program were performed at 20 inches of vacuum, which is typically used in photolith steps. All measurements were made with the vacuum chuck surface levelled with no attempt to account for wafer taper.

The high and low spots were identified, and fringes counted down from high toward low. The fringe count was confined to the center part

a)



b)



c)



Figure 1. SOS wafer flatness measurement under a) 5 inches of vacuum, b) 25 inches of vacuum, c) calibration wedge.

of the wafer, discounting rounding of the wafer edge where devices are not usually fabricated. There is some operator judgment involved in identifying the central region of the wafer. In Figure 2a, most of the wafer shown is very flat, with some edge rounding at the left side. The closely spaced group of fringes at the left is not counted. Figure 2b shows a common configuration among the vendor wafers. The lower half of the wafer is very flat, but the upper half shows closely spaced parallel fringes indicating taper. This wafer has a "peaked-roof" shape with two planar regions at a slight angle to each other. The close fringes definitely lie within the central area of the wafer and must be counted. It would be impossible to align this wafer to get perfect focus on both halves in a single, whole-wafer mask process. However, using a DSW projection aligner, excellent focus could be obtained on each half by realignment during each individual chip exposure. The only problem would arise with chips that straddle the "peak" of the roof shape. Finally, Figure 2c shows a wafer which is more uniformly tapered across an entire diameter. There were only a few wafers with such an evenly spaced pattern of parallel fringes.

The distribution of wafer flatness data is shown in Figure 3. The mean value of flatness is $4.05\text{ }\mu\text{m}$ and the rms variation about the mean is $1.83\text{ }\mu\text{m}$. The range of variation is from 1.37 to $9.06\text{ }\mu\text{m}$. All of the wafers met the specification of $10\text{ }\mu\text{m}$ flatness, although many would have shown a greater variation if the edge rounding had not been neglected.

2.2 Wafer Bow

Wafer bow is defined as the deviation from flatness of the wafer surface when the wafer is unconstrained. For measurements of bow, the wafer is held by a vacuum fixture of small diameter located at the center of the wafer. The wafer is free to assume its natural shape without being distorted by the small vacuum contact area. Wafer bow is expected to be a yield factor because of the importance of wafer shape in various processing steps. The shape of a wafer determines the

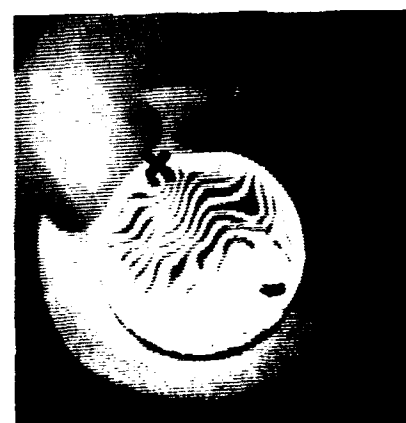
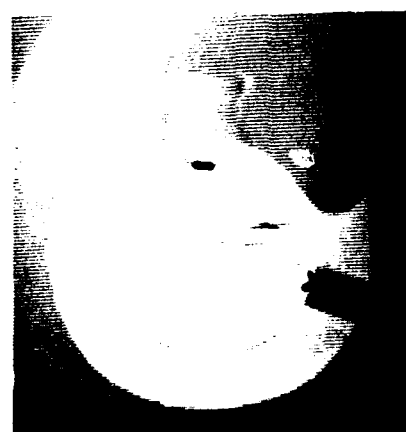


Figure 2. Wafer flatness interferograms -- 0.67 microns per fringe:
 a) very flat wafer, b) "roof-shaped" wafer, c) tapered wafer.

Curve 746180-A

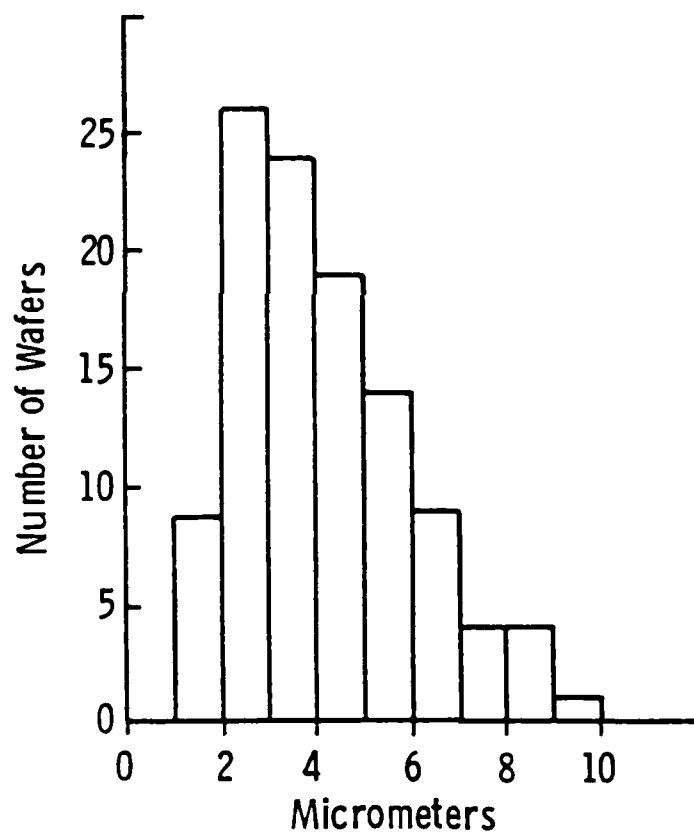


Figure 3. Distribution of wafer flatness data from interferograms.

contact area and the proximity of the wafer to the supporting structure when the wafer is laid flat on a heated surface for process steps such as oxidations. The contact area and proximity to the heated surface will affect the temperature distribution in the wafer, and so will affect the uniformity of the result of the process step. Nonuniform temperature distributions can also contribute to cracking of the wafer due to thermal stress.

There are several causes of wafer bow. Due to the different thermal expansion coefficients of silicon and sapphire, the silicon layer is placed in compression in cooling from the growth temperature of the epilayer. For isotropic substrate and epilayer, this would give a wafer which is convex viewed from the epilayer side, with approximately spherical shape near the center of the wafer. The substrate, however, is not isotropic. Because of the hexagonal crystal structure of sapphire, the elastic response of the substrate is a function of direction. As a result, the wafers are not spherical but typically show a symmetry axis which lies along the c-axis projection in the plane of the wafer. The shape of the wafer is also affected by residual stresses which may exist in the substrate depending on the fabrication processes involved. Wafer bow measurements were taken on a Tropel Model 9000 wafer flatness analyzer. This is an optical interferometric instrument with adjustable sensitivity.

The wafer is held by vacuum on a "wafer-bow chuck" supplied by Tropel. The vacuum mount consists of a single cup about 0.25 inch in diameter. Aside from contact with this cup, the wafer is not in contact with any other surface on the vacuum chuck or the surface plate.

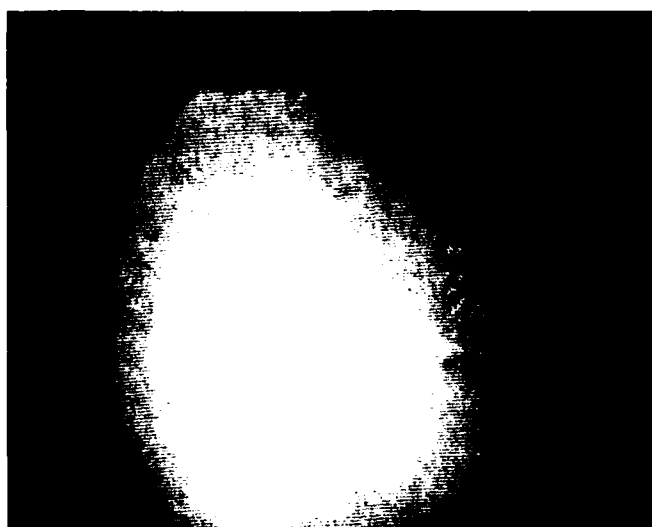
The wafer shape measured this way is the free or unconstrained shape, subject only to the vacuum pressure at the center and distortions due to gravity. Examination of fringe patterns shows that no change is visible when the vacuum is varied from 5 to 25 psi, and the influence of gravity is assumed to be negligible.

Typical interferograms are shown in Figure 4. Wafer W37F is approximately spherical in shape. The surface is convex when viewed from the side of the epilayer, as determined by observing that the fringes run toward the edge of the wafer when pressure is applied to the mounting fixture. The fringe sensitivity for this interferogram was $4.75\text{ }\mu\text{m}$ per fringe, giving a total bow of $19\text{ }\mu\text{m}$ from the highest point to the edge. Also shown in Figure 4 is an interferogram of wafer W41F. This wafer has a saddle shape with two high spots diametrically opposite each other, and two low points at the extreme of a diameter about 90 degrees away from that connecting the high spots. The total range from high to low is 4.5 fringes, or $21\text{ }\mu\text{m}$. The diameter connecting the high spots coincides with the c-axis projection in the plane of the wafer. Evidence for the alignment of this symmetry axis is presented in the section on the angular dependence of UV scattering (Section 3.2.5).

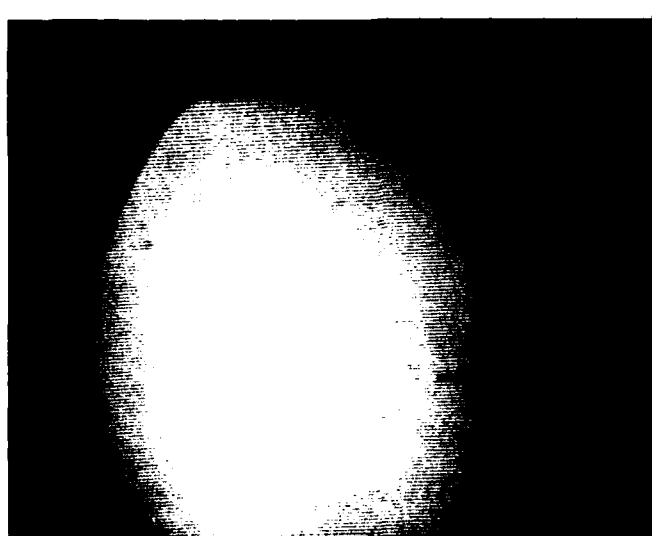
The range of variation in wafer shape is illustrated in Figure 5. The wafer in Figure 5a is practically flat, while the wafer in Figure 5b is strongly warped, with a total bow of $25\text{ }\mu\text{m}$. The distribution of the bow data is shown in Figure 6. The mean value is $5.4\text{ }\mu\text{m}$ with an rms variation of 5.2 above the mean. The range of variation is from 2.4 to $25.3\text{ }\mu\text{m}$. All of the wafers met the specification of less than $50\text{ }\mu\text{m}$ or bow.

2.3 Epilayer Thickness Measurements

The thickness of the silicon epilayer is one of the parameters specified when ordering SOS wafers. Deviations from the specified limits on layer thickness can reduce eventual device yield. Various process steps, such as deep implants to suppress back-channel leakage, are sensitive to layer thickness and will not be effective in wafers that do not meet the specification. In this section we describe the characterization of vendor wafers with regard to layer thickness. Results are presented for the average layer thickness on each wafer, the

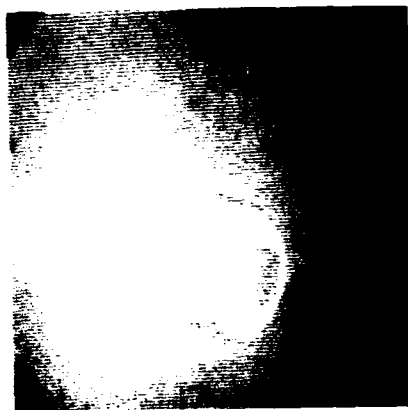


W37F



W41F

Figure 4. Interferograms showing the unconstrained shapes of wafers W37F and W41F; the calibration is $4.75 \mu\text{m}/\text{fringe}$.



A



B

Figure 5. Wafer bow interferograms -- 4.8 microns/fringe:
a) least bowed, b) most bowed.

Curve 746181-A

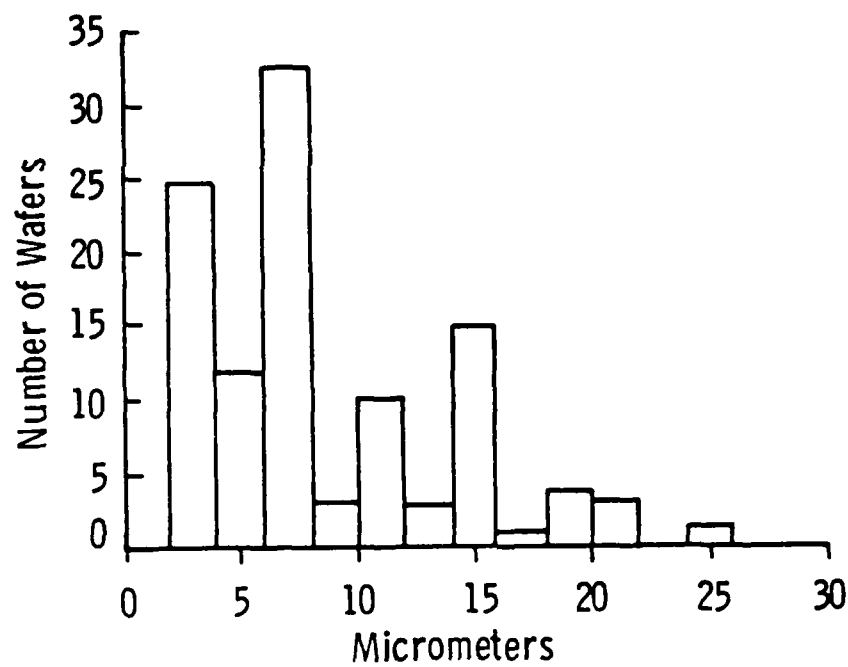


Figure 6. Distribution of wafer bow data from interferograms.

range of variation of layer thickness on each wafer, and the number of measurements out of the specified range of variation. The method chosen for silicon layer thickness is based on wavelength-dependent reflection, a nondestructive technique suitable for screening on all wafers. The instrument, an Applied Materials Reflectometer I, directs white light onto a spot about 0.25×5.0 mm in size on the wafer. Reflected light is focussed onto the slit of a monochromator to provide wavelength selectivity. The monochromator is adjusted for successive local minimums in reflectivity, and the wavelengths are read on a calibrated dial. Maximum or minimum reflectivity occurs at wavelengths given by

$$\frac{4nd}{\lambda} = m + \frac{S_1 - S_2}{\pi} \quad (1)$$

where n is the index of refraction of the silicon layer, d is the thickness of the layer, λ is the wavelength in air, and S_1 and S_2 are phase angles for reflections at the air-silicon and silicon-sapphire interfaces.⁽¹⁵⁾ The minimum reflectivity is obtained when m is an even integer, and maximum when m is odd. The phase angles are given by

$$\begin{aligned} \tan S_1 &= \frac{2k}{n^2 - 1 + k^2} \\ \tan S_2 &= \frac{2k n_s}{n^2 - n_s^2 + k^2} \end{aligned} \quad (2)$$

where k is the absorption of the silicon film and n_s is the index of the sapphire substrate.⁽¹⁵⁾ Computation of the expected values of S_1 and S_2 in the wavelength range of interest, using n and k values from Verleur,⁽¹⁶⁾ show a negligible contribution of 2 nm or less from this term. The layer thickness is thus given with sufficient accuracy by

$$d = \frac{m\lambda}{2n} \quad (3)$$

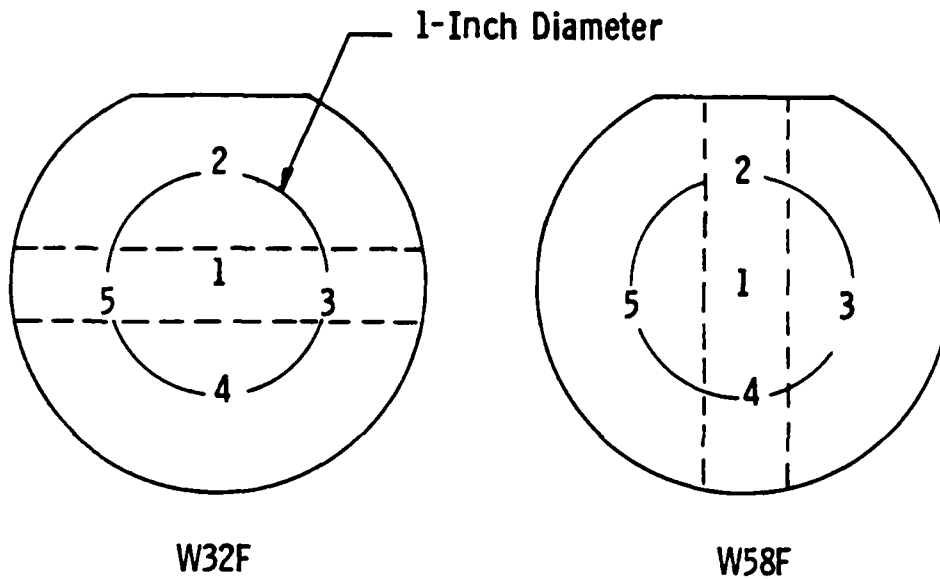
where m is an integer for the order of the reflectivity minimum.

To make use of Equation 3, the proper order number m must be known, which is determined by testing for consistency in a given data set. Typically about six reflection minimums can be observed which represent six independent thickness measurements via Equation 3 for six consecutive increasing values of m , starting from a minimum value m_0 at the longest wavelength. For a given value of m_0 , a computer program is used to compute the six resulting values of d from Equation 3, taking into account the wavelength dependence of n by means of a polynomial fit to the data of Huen.⁽¹⁷⁾ The correct value of m_0 is assumed to give the lowest sample standard deviation of the six thickness values so computed. Once m_0 is identified, the average value of the six computed thicknesses is reported as the measured layer thickness. The sample standard deviation reflects the statistical uncertainty in the thickness. Possible sources of error are inaccurate reading of the wavelength, neglect of the interface phase angles, incorrect index of refraction at wavelength, and local inhomogeneities in the sample. The observed standard deviations are typically about three percent of the layer thickness, so the statistical uncertainty is not a serious problem.

The uniformity of the layer thickness is assessed by repeating the measurement at five points on the wafer. One point is at the center of the wafer, while the other four points are spaced 90 degrees apart on a circle of one-inch diameter, as shown in Figure 7.

In order to verify the accuracy of this technique, a direct comparison has been made with a mechanical layer-thickness measurement. Two SOS vendor wafers were chosen for the comparison experiment. The original epilayer-thickness data for these wafers are shown in Figure 7 along with the location of the measurement points. Examination of the data shows that wafer W32F has a substantial thickness variation along the line connecting points 5, 1, and 3, and W58F has a thickness variation along the line 2, 1, and 4. These wafers, selected as among the worst of the vendor wafers in thickness uniformity, were used to verify the degree of thickness variation and to

Dwg. 7755A15



Initial Layer Thickness Measurements

Location	W32F	W58F
1	508	506
2	526	478
3	476	507
4	498	539
5	538	500

Figure 7. Initial reflectivity data for selected vendor wafers showing measurement locations and orientation of etched stripes.

get more detailed data on whether the layer thickness varied smoothly or irregularly across the wafer.

Both wafers were masked by painting black wax over the surface, leaving a strip exposed about 8 mm wide. The silicon in the exposed stripe was then removed using a nitric, acetic, hydrofluoric acid etch. The orientations of the etched stripes are shown in Figure 7. Epilayer-thickness measurements were made along the edges of the stripes by taking surface-profile traces with a Talystep profilometer. A typical trace is shown in Figure 8. The precision of this measurement is estimated at about 6 nm. After each trace was taken, a mark was made on the exposed sapphire to indicate the position of the measurement. The wafers were then placed in the optical reflectometer, where epilayer-thickness measurements were made as closely as possible to the marks. The long axis of the illuminated area was placed perpendicular to the edge of the etched stripe to minimize the thickness variation within the measured area.

The results of this comparison are shown in Figure 9. The substantial thickness variation detected by the original reflectivity-point measurements is confirmed. Wafer W32F shows 10% variation over a one-inch range based on the detailed measurements, while the original data indicated a 12% variation between points 2 and 4. Wafer W58F shows 11% variation over a one-inch range compared to 12% between points 5 and 3 in the original data. The Talystep data agree well with the corresponding reflectivity data. The reflectivity data for W32F average to 1.9 nm less than the Talystep data, with 2.3 nm rms variation about the mean. Wafer W58F showed reflectivity data averaging 5.9 nm less than the Talystep data, with 3.2 nm rms variation. There is no probable systematic error on wafer W58F since there is little thickness variation in the direction perpendicular to the stripe. However, in wafer W32F there is a thickness change of 28 nm between points 2 and 4 as shown in Figure 7. If the thickness variation is approximately linear, this reduces to 1.1 nm of thickness change per 1 mm of displacement along the line joining points 2 and 4. Because of the size of the illuminated

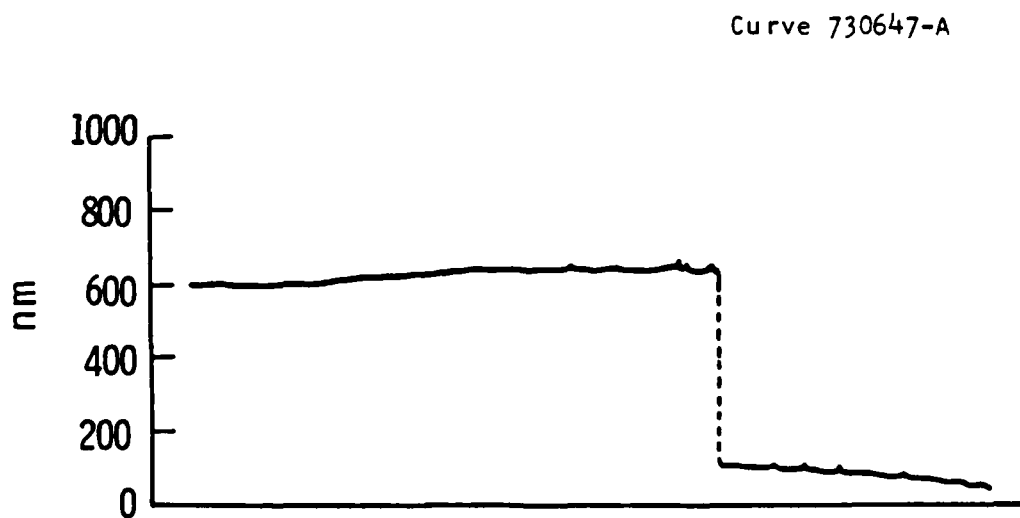


Figure 8. Talystep surface profile of measurement point on W58F; height of step indicates thickness of epilayer.

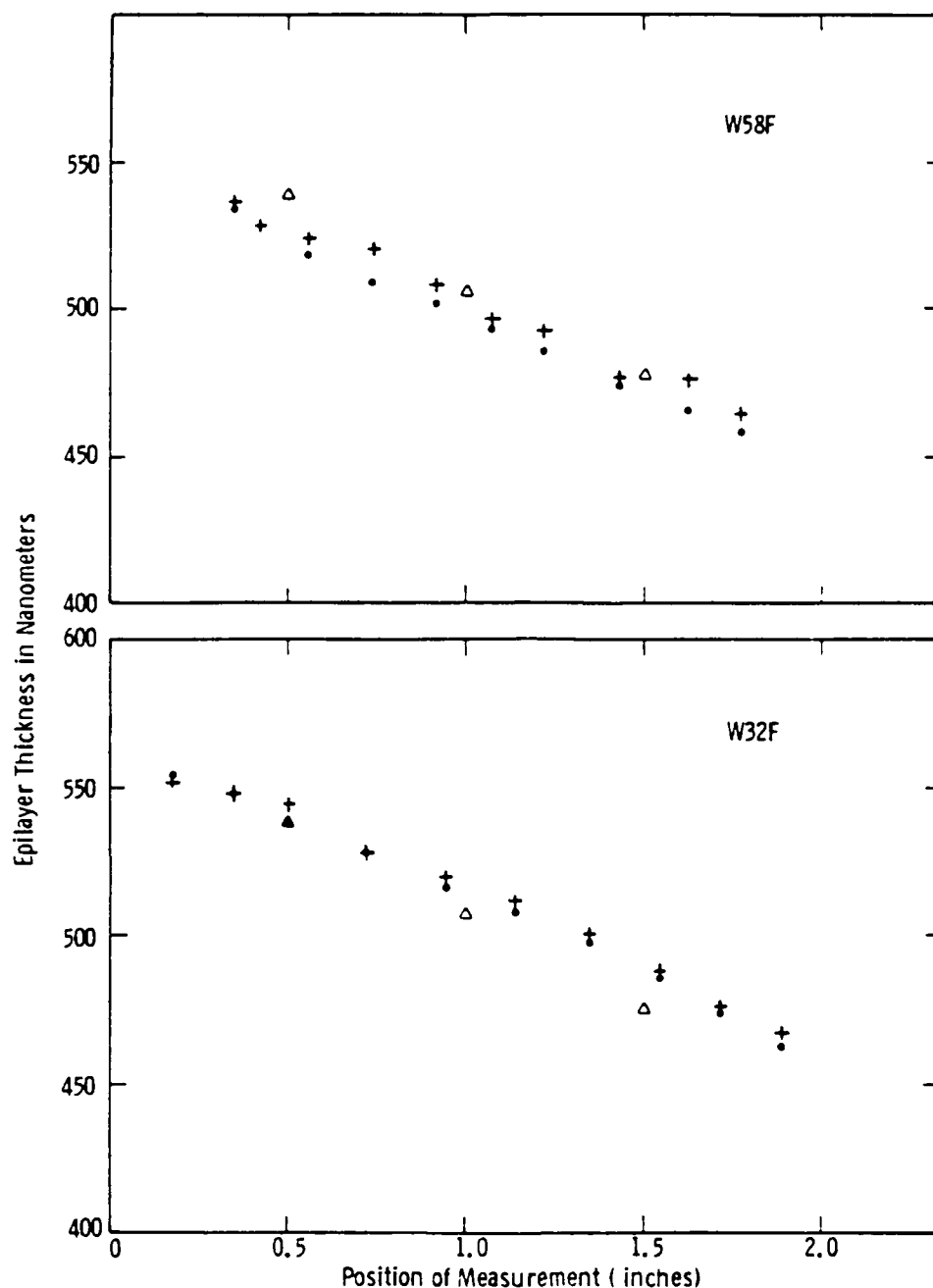


Figure 9. Epilayer thickness versus position along etched stripe in wafers W32F and W58F.

Δ = initial measurement by optical reflectivity
 + = Talystep data
 o = reflectivity data

area, the center of the measurement region in the reflectometer is displaced about 4 mm toward point 4 from the edge of the stripe. Thus, one would expect the reflectivity data to lie 4.4 nm below the Talystep data, whereas they actually lie 1.9 nm below. The net discrepancy then is +2.5 nm for W32F and -5.9 nm for W58F, taking into account the lateral-thickness gradients. These discrepancies compare with the estimated 6 nm precision of the Talystep measurements and the 3.2 nm average sample variance for the reflectivity measurements. Based on these results, we consider the reflectivity technique to give the silicon epilayer thickness an accuracy of 6 nm or better, or about 1% of the epilayer thickness. With observed epilayer-thickness variations of typically 5% or so, this accuracy is considered adequate for the purposes of this program.

The results of the measurements are shown in Table 3 and the associated histograms. The specification on epilayer thickness for the lots ordered from the vendor was 500 nm with a 10% tolerance range. The specified thickness and the allowable range are shown on line 1 of Table 3. The results of our measurements show a mean value of 503.9 nm and a range from 448.6 to 542.6 for the average thickness based on five measurement points per wafer. Out of 110 wafers, only 2 failed to meet the specification by being too thin. The worst case corresponds to a 10.3% deviation from the specified value, only very slightly beyond the specified 10% tolerance range. As shown in Figure 10, the distribution of epilayer thickness shows two peaks at about 530 and 470 nm. This distribution is also reflected in the 25.6 nm rms variation about the mean of the average layer thickness, as shown in Table 3.

For the wafers used in this program, the vendor supplied thickness data on each wafer. According to the vendor, the mean layer thickness is 520.7 nm and ranges from 458.5 to 553.5 nm. There are five wafers out of specification by being too thick, with the worst case corresponding to 10.7% deviation from the specified value. The vendor data also show a distribution with two peaks, as shown in Figure 11.

Table 3
Epilayer Thickness Data

<u>Item</u>	<u>No. of Points</u>	<u>Mean</u>	<u>Range</u>		<u>RMS</u>	<u>Out of specification</u>	
			<u>min.</u>	<u>max.</u>		<u>low</u>	<u>high</u>
Specified Layer Thickness	--	500	450	550	-	-	-
Average Epilayer Thickness	110	503.9	448.6	542.6	25.6	2	0
Vendor Epilayer Thickness	110	520.7	458.5	553.5	27.5	0	5
Difference Between Vendor and Westinghouse Data	110	16.9	- 7.2	83.4	10.4	-	-
Local Thickness	550	503.9	438	585	29.8	9	30
Thickness Variation on Single Wafer	110	39.8	10	85	17.2	-	35
RMS Variation on Single Wafer	110	14.0	4.2	38.0	6.0	-	-

Curve 744633-A

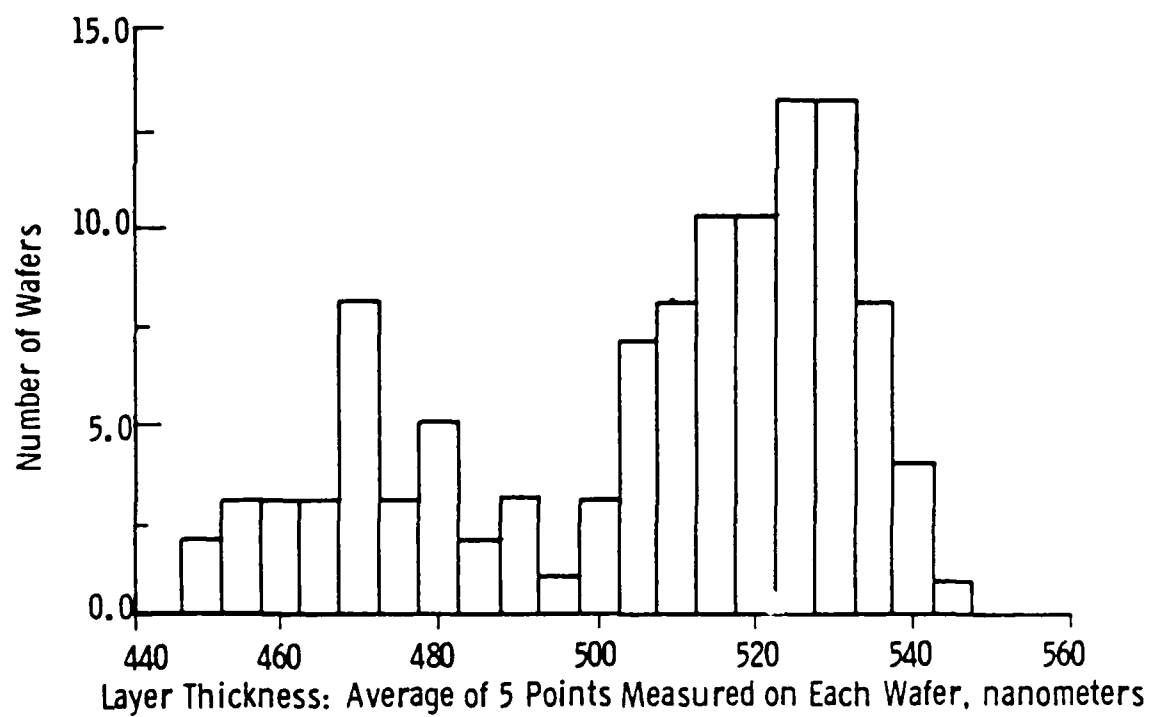


Figure 10. Distribution of average layer thickness.

Curve 744636-A

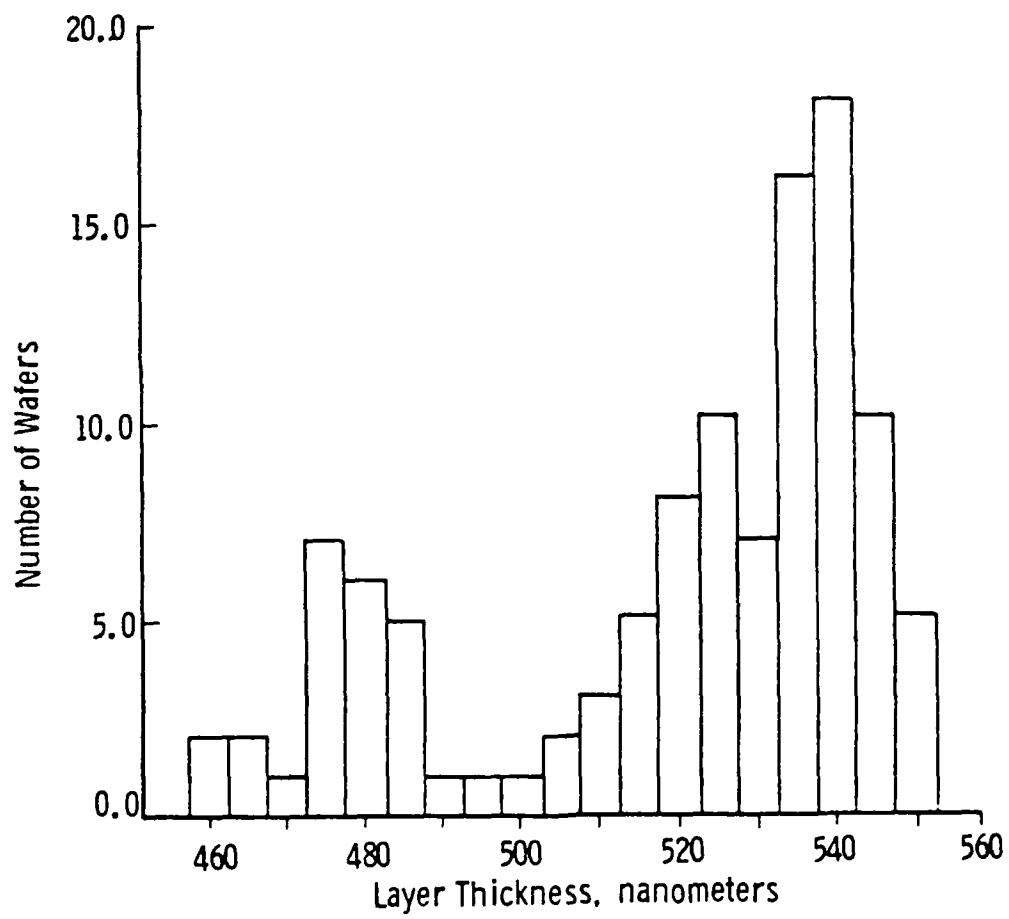


Figure 11. Distribution of vendor data on layer thickness.

The difference between the vendor data and our data for each wafer is summarized in Table 3. The mean deviation is 16.9 nm and the range is from -7.2 to 83.4. However, Figure 12 shows that most of the deviations are clustered closely about 20 nm and only a few exceptional cases account for the wide range. This indicates a systematic difference in calibration of thickness measurements at Westinghouse and at Union Carbide. Since we have verified our measurement procedure by comparison with profilometer data, we will use our data for all further comparisons.

The thickness was measured at five points, comprising a data set of 550 points. As shown in Table 3, the local thickness data range from 438 to 585 nm, with 9 points lying below the spec range and 30 points above. All of the measurement points lie within 0.5 inch of the center of these 2-inch diameter wafers. This increased range of the local thickness indicates a possible problem in the uniformity of epilayer thickness on a single wafer. The distribution shown in Figure 13 is not as cleanly separable into two peaks as is the wafer average data. Considering the thickness variation on each wafer, taken as the maximum range among the five points measured, we find that the mean value is 39.8 nm, as shown in Table 3. Thus, there is typically about an 8% variation in layer thickness within the central region of a single wafer. There are 35 wafers, out of 110, in which the thickness variation exceeds 50 nm, or 10% of the target thickness. This demonstrates a problem in maintaining wafer uniformity within bounds of the specification. The histogram in Figure 14 shows a broad distribution of thickness ranges on a single wafer, with relatively few wafers having uniformity better than 4%. The rms variation in layer thickness on a single wafer is also summarized in Table 3 and shown in Figure 15.

2.4 X-ray Orientation and Rutherford Backscattering

Two SOS wafers were submitted for X-ray diffraction analysis for the crystal orientation of the sapphire substrate. The first objective was to verify the orientation with respect to the specification of

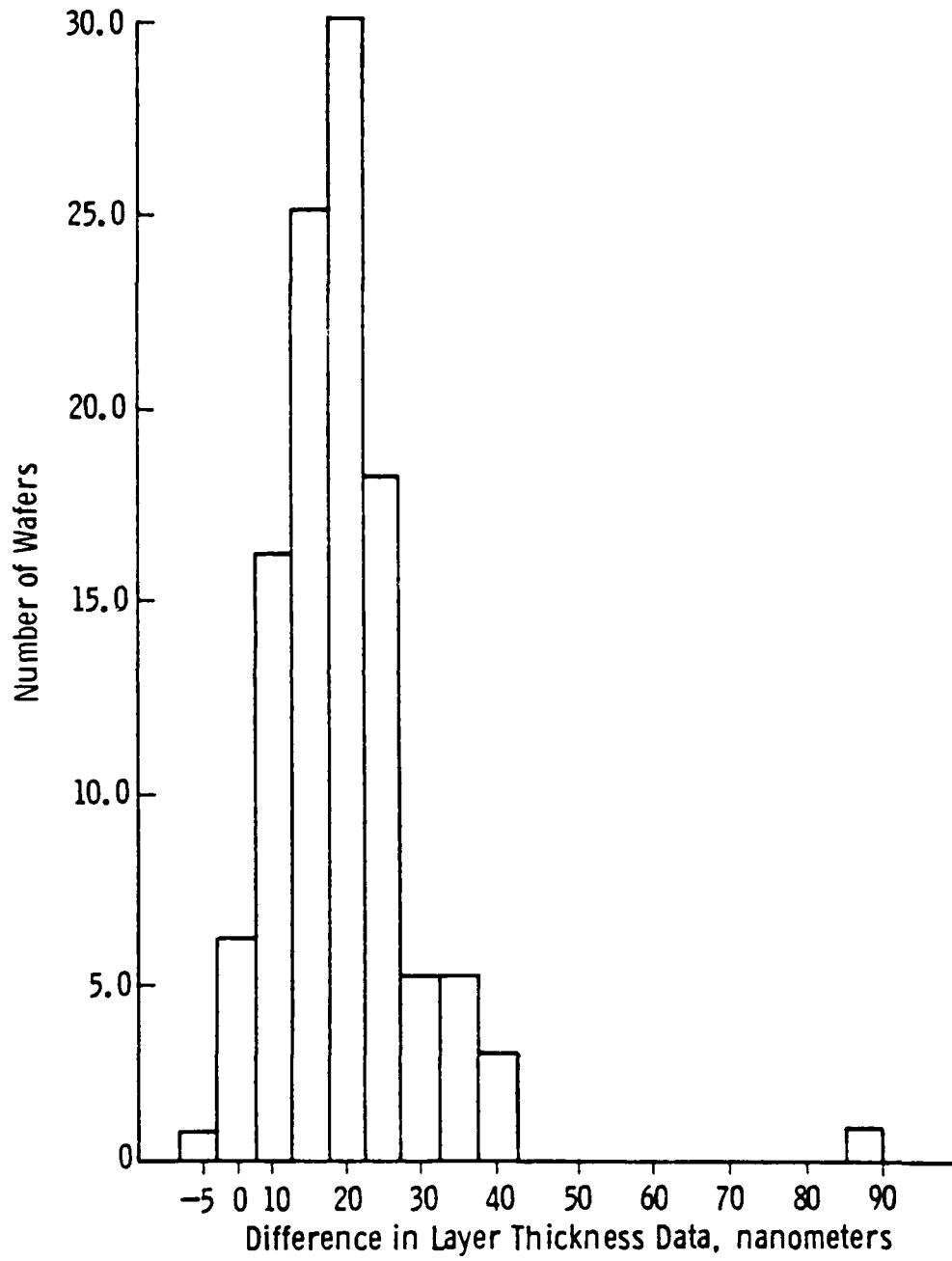


Figure 12. Distribution of the difference between vendor layer thickness data and Westinghouse data for 110 wafers.

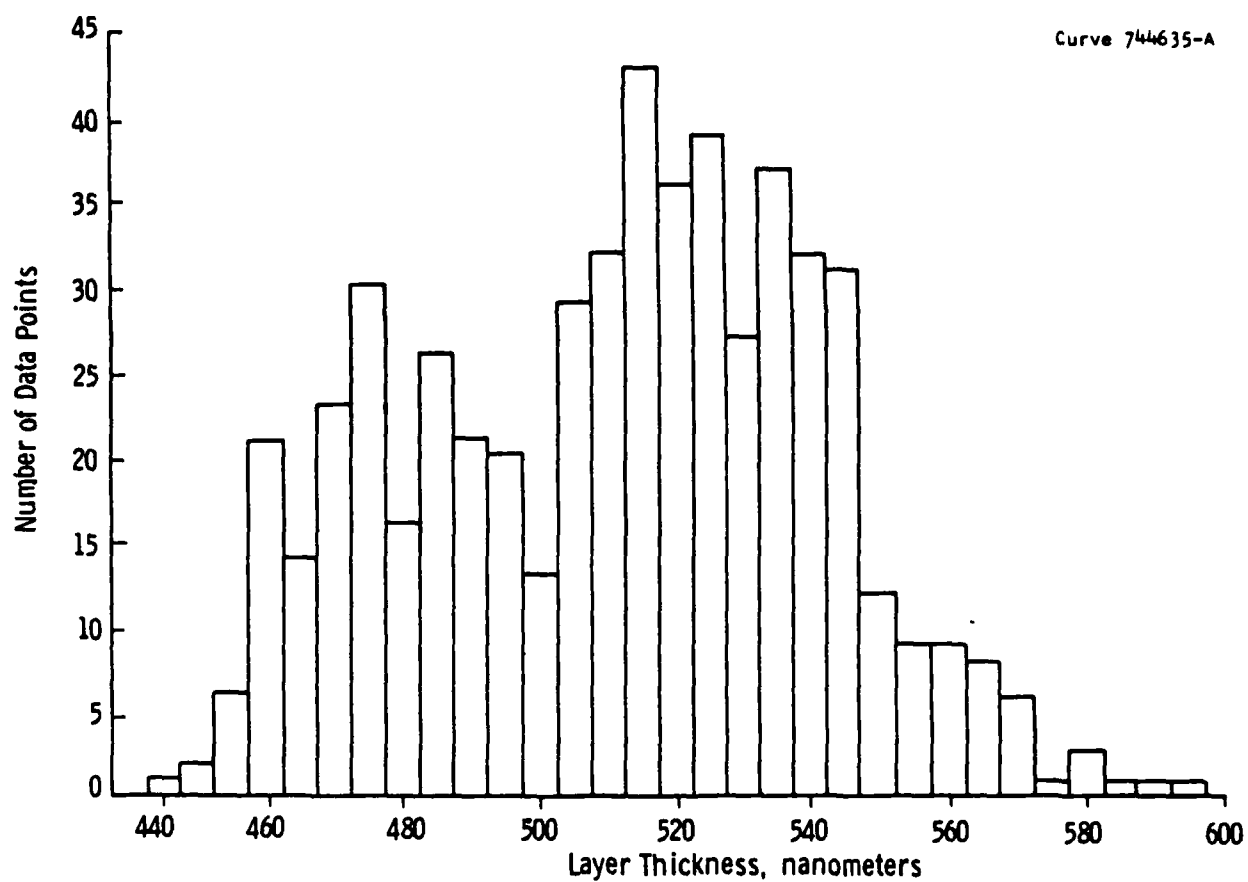


Figure 13. Distribution of layer thickness measurements of 550 data points on 110 wafers.

Curve 744634-A

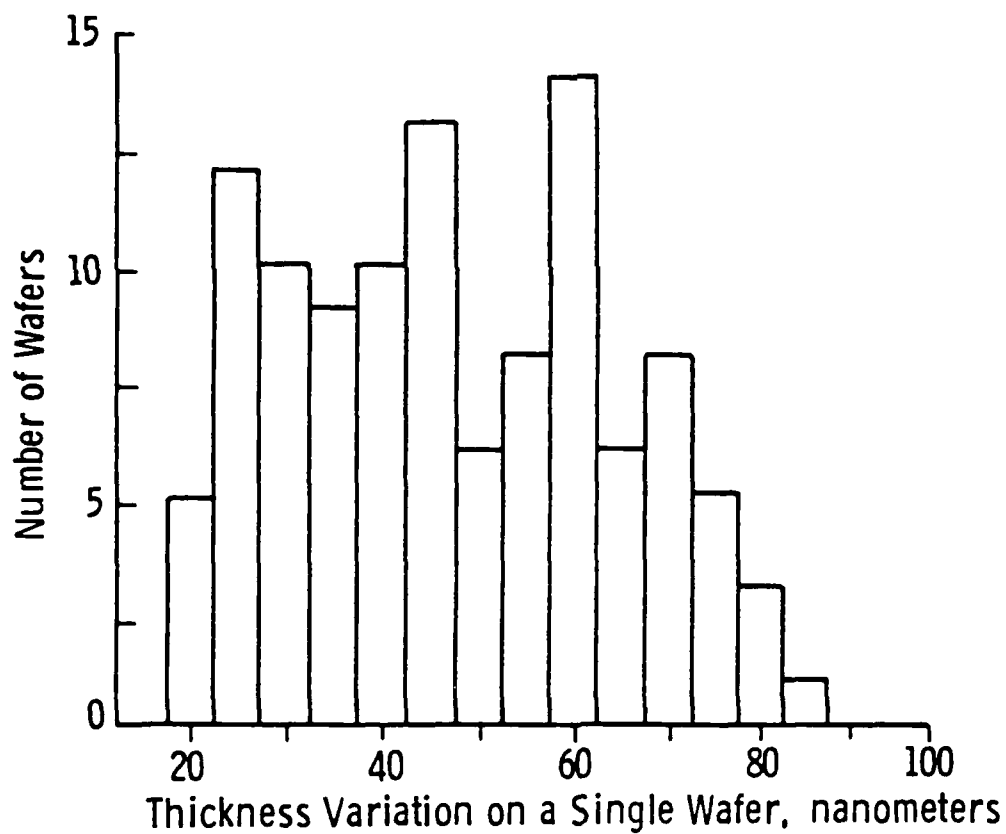


Figure 14. Distribution of thickness variation.

Curve 744632-A

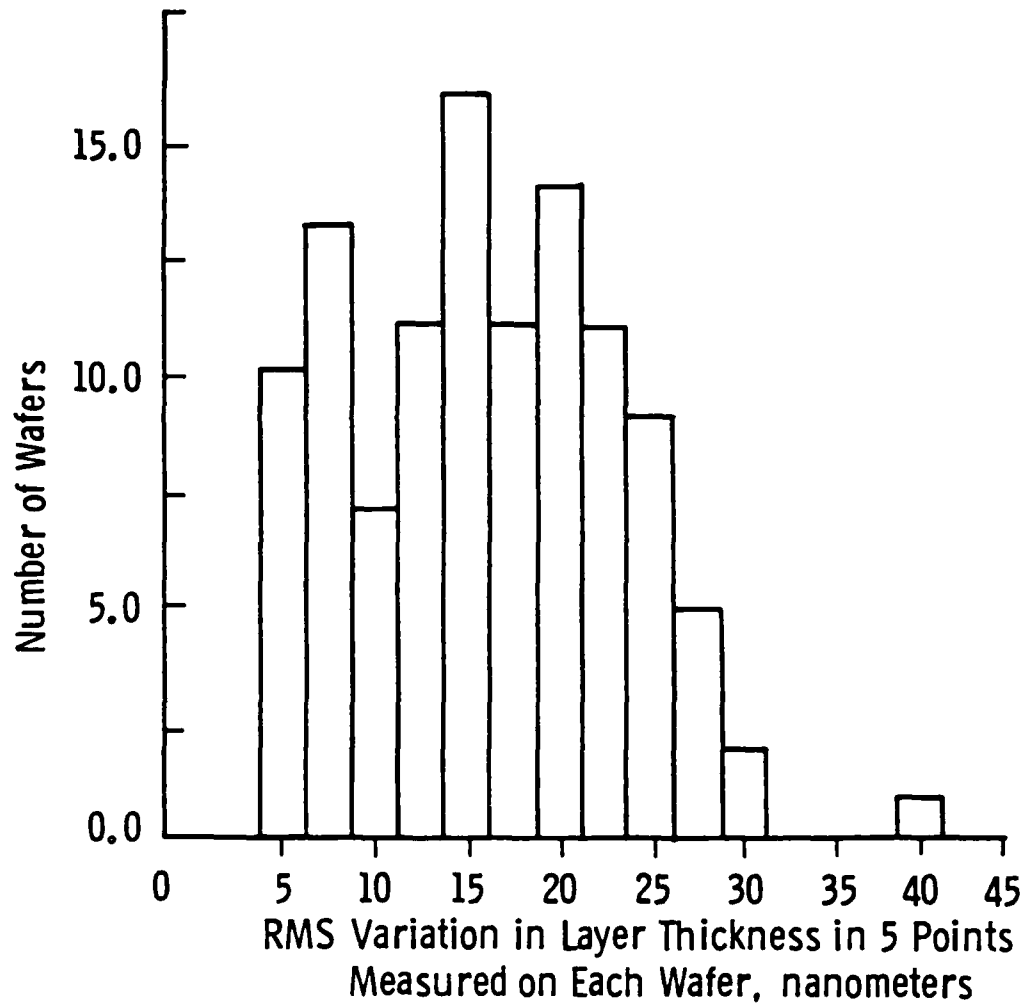


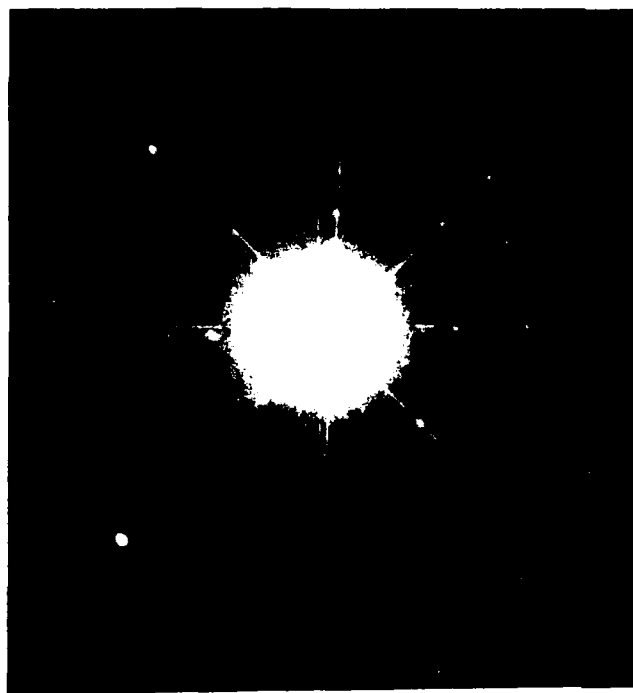
Figure 15. Distribution of the rms variation of layer thickness on single wafers.

± 2 degrees from 1102 plane. The second objective was to determine whether the direction of peak scattering (see Section 3.2.5) aligns with the crystal orientation of the substrate.

The wafers were placed in a 2-axis goniometer. The surface was adjusted to be perpendicular to the incoming beam of X-rays by optical alignment of a laser beam colinear with the X-ray beam. The resulting diffraction patterns are shown in Figure 16. Analysis of the deviation from symmetry about the center of the beam shows a 0.5° misorientation for W82F and 1.0° for W78F. Both of the orientations are within specifications.

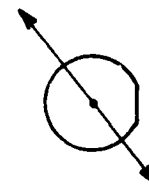
Close inspection of the diffraction patterns confirms that the substrates do not exhibit four-fold symmetry. The photo for wafer W82F must be rotated by 90° to reach the same pattern as W78F. This corresponds to a difference in wafer position as shown in the drawings in the figure. This is consistent with the 90° shift between the angular orientations of the peaks of UV scattering from these wafers. The approximate angular orientation of the major optical scattering peaks is shown in the figure. The specification on wafer orientation requires that the sapphire c-axis projection lie 45° away from the flat on the finished wafer. The difference between W78F and W82F appears to be a $+45^\circ$ location of the c-axis for one wafer and a -45° location from the flat for the other. This is probably due to some of the substrates being flipped over before the final polishing operation.

The location of the c-axis was determined on wafer W61F by tilting the wafer by the nominal amount (58° away from normal incidences in a plane 45° away from the flat) required to obtain a symmetrical diffraction pattern. The results are shown in Figure 17. The two patterns correspond to the orientations shown in the drawing. The symmetric pattern in Figure 17a shows that in this sample the c-axis projection is 45° counterclockwise from the flat. This wafer was the Type I scattering pattern versus rotation angle as explained in Section 3.2.5.



a

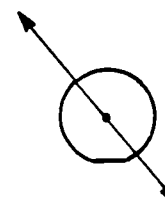
Wafer
Orientation



W78F



b



W82F

Figure 16. X-ray diffraction patterns for two SOS wafers. The relative orientations of the wafers are shown as well as the angular orientations of the peaks of optical scattering.



a



b

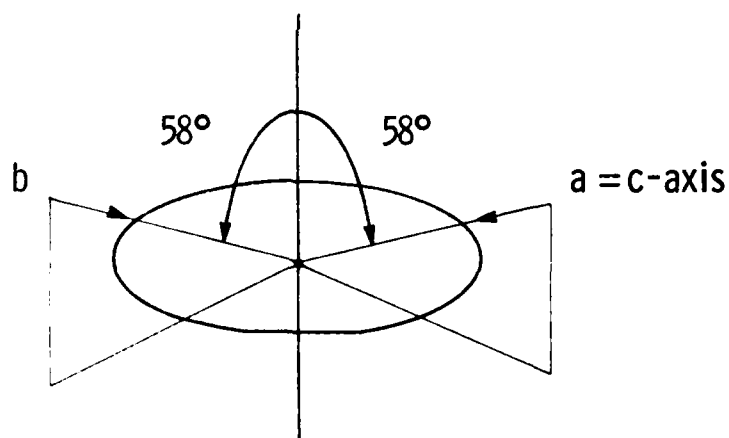


Figure 17. X-ray diffraction pattern for WOLF; the X-ray beam directions are shown in the tracing. For this Type I water, the a -axis is shown to the left counterclockwise from the water flat.

2.4.1 Rutherford Backscattering Measurements

Selected SOS wafers have been characterized by Rutherford backscattering (RBS) analysis. This characterization reveals the crystal quality as a function of depth between the surface of the silicon epilayer and the interface with the sapphire substrate.

RBS is essentially a nuclear scattering process. Helium nuclei are commonly used as the probe species. A beam of high-energy He^+ ions is generated in a linear accelerator such as a Van de Graaf machine. The ion beam is directed onto the sample, where the energetic He nuclei scatter from the nuclei of atoms in the sample by Coulomb repulsion. If the He ion happens to strike an atom at the surface of the sample, the energy of the backscattered He nucleus is given by the mass ratio of the He and the scattering atom and the angle between the incident beam and the path of the scattered He ion. The detector is located in a position to select only He ions scattered at a particular angle, so the energy for surface scattering is determined only by the mass ratio. The detector gives an output pulse amplitude proportional to ion energy, and the output pulses are sorted according to amplitude by a multichannel analyzer. The accumulated count in each channel indicates the number of ions of given energy detected during the run.

Only a small fraction of the incident He ions are scattered right at the surface. Most of the ions in the beam penetrate some distance into the sample before they encounter a nucleus closely enough to cause a backscattering event. While an ion is moving inside the sample, it loses energy in small increments by interactions with the electrons in the sample. A backscattered ion loses energy both going into and coming out of the sample. The energy loss is approximately a linear function of distance travelled in the sample, providing an energy versus depth scale for scattering events from a given type of nucleus.

The general features of an RBS spectrum can now be interpreted. In a display of the number count of scattering events at a given energy versus the energy, there are no events above a threshold

energy. At the threshold, which is the energy for surface scattering, there is a sharp increase in the number of events. At lower energies, the count of events varies smoothly as a function of the electronic energy loss versus depth, and the scattering cross section versus ion energy. If the sample is doped with heavy atoms, such as arsenia in silicon, scattering events from the heavy atoms will stand out at higher energy than the silicon. Lighter dopants, such as boron, will cause peaks in the midst of the scattering from silicon which lie at lower energy.

The scattering as described above applies to amorphous material, or at a random incidence angle of the ion beam onto a crystal. When the beam is precisely aligned with a crystal axis, channeling may occur. Channeling is due to the long range order of the arrangement of atoms in a perfect crystal. Along the 100, 111, and especially the 111 axes of a silicon crystal, the crystal structure creates open channels of indefinite length where the density of nuclei is zero. An ion entering such a channel will have a very low probability of scattering and will penetrate much farther into the crystal. The scattering yield for a beam aligned with a crystal axis is therefore very much reduced. The ratio of the reduced scattering for an aligned beam to the scattering for a random beam indicates crystal quality. In a highly perfect crystal, the ratio of channeling yield to random yield is typically a few percent. Crystal defects, such as dislocations, grain boundaries, and stacking faults, place atoms in the channels, increasing the channeling yield. While it is not possible to determine which type of defect causes the increased yield, the total yield can serve as an average quality index. Furthermore, because of the energy loss versus depth calibration, the crystal quality can be determined as a function of distance from the surface.

RBS measurements have been made on several vendor and Westinghouse wafers. The vendor wafers include W18F and W32F, which were known to have nonuniform epilayer thicknesses, and W44F, which was very uniform according to epilayer thickness data. These samples were

selected for comparison of the crystal quality of uniform and nonuniform wafers. The epilayer thickness was the best available indicator of uniformity. UV haze data for these wafers were not available when the selection was made. Wafer 32F had been etched and profiled for confirmation of the epilayer thickness variation, as reported in Monthly Status Report #7. The Westinghouse wafers W301F and E31F were low-temperature epilayers. The preliminary UV haze measurements on both of these wafers were much higher than any of the vendor wafers.

The samples were prepared by scribing and breaking pieces about 1 cm square from each wafer since the goniometer used for precise channel alignment would not accommodate entire wafers. The samples were probed with a beam of 1.5 MeV 4He^+ ions. The scattering data were acquired by a computerized data-handling system where the data were stored for normalization and comparison. In the display figures, the scattering counts for the silicon epilayer with the random incidence angle were normalized to represent a yield level of one. All channeling data were normalized with respect to the random yield.

The RBS spectrum for sample W18F is shown in Figure 18. The random yield rises rapidly from zero to one at the energy for surface scattering. The onset of random scattering also serves to locate the surface for the depth scale. The SOS channeling yield also shows a sudden onset for surface scattering, and then a steady increase in normalized scattering until the interface is reached at an indicated depth of 0.43 microns. There is a decrease in scattering yield at 0.43 microns because the material underlying the silicon is composed of lighter elements, aluminum and oxygen. The scattering spectrum for indicated depths greater than 0.43 microns contains information only about the sapphire substrate and is therefore only of slight interest.

Figure 18 also shows the data for a good 100 silicon crystal. The silicon spectrum shows a high-surface scattering peak followed by a much lower channeling yield. The surface peak is due to scattering of ions which do not happen to enter channels and to any residual surface

Curve 739205-A

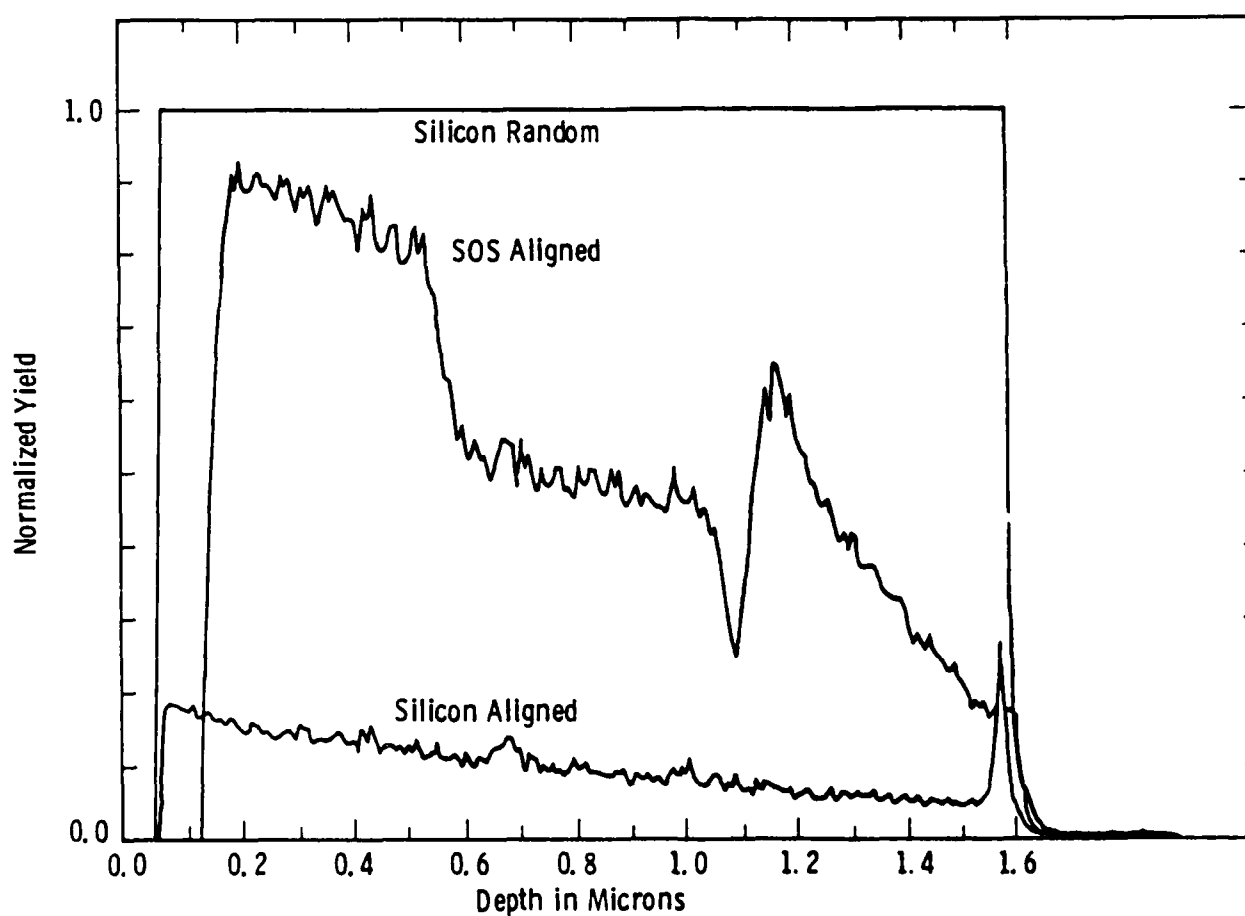


Figure 18. Rutherford backscattering spectrum from vendor wafer W18F.

damage after polishing. Except for the surface peak, the silicon crystal channeling yield is substantially less than the SOS yield at all depths. A comparison of the normalized channeling yields of the silicon reference sample and the SOS will provide a quantitative index of crystal quality.

The channeling spectrum of W18F is typical of the vendor wafers in its general features. The scattering at the silicon-sapphire interface is very high, indicating the poor crystal quality of that region of the epilayer. The scattering decreases toward the surface, more rapidly near the interface, and less rapidly near the surface. There is a relatively constant scattering region very near the surface. Some of the vendor wafers show a surface scattering peak, but the amplitude of the peak is much smaller than that of the silicon reference sample. These spectra for the SOS wafers are characterized numerically by two parameters: the surface and interface scattering yields. The interface scattering yield x_i is simply the maximum normalized yield at the interface. In cases where the residual noise in the spectrum appears to give a spurious peak at the interface, a visual estimate of the average level at the interface is taken. Since this is a normalized scattering yield, it is a fraction, typically about 0.6, which can also be expressed as a percentage of the random yield. The surface scattering x_o is taken as the normalized scattering yield near the surface, neglecting any surface peak that may be present. This number represents the lowest yield that is actually observed near the surface, not an extrapolation of the decreasing curve to the surface. The surface yield for the silicon reference wafer is determined in the same way, neglecting the surface peak. The reference interface yield is simply the observed yield at a depth in the silicon crystal corresponding to the SOS interface depth. The silicon reference wafer interface yield will vary somewhat since the interface depth varies with epilayer thickness.

The results show that the vendor wafers are reasonably uniform in crystal quality. Two samples cut from W22 are shown in Table 4,

Table 4
Rutherford Backscattering Results

CHANNELING YIELDS NORMALIZED TO RANDOM SILICON YIELD

Sample		x_0	x_i	$x_i(\text{SOS})/x_i(\text{Si})$
W18F		.16	.63	9.4
W32F-1	location 1			
"	2	.13	.56	8.3
"	3	.10	.55	8.2
W32F-2	location 1	.00	.58	8.7
"	2	.09	.56	8.3
"	3	.09	.56	8.3
W44F		.11	.55	9.3
W301F		.80	1.00	12.3
W312F		.89	1.00	17.0
Silicon Standard Wafer		.04	0.08-0.11	

where data from three distinct areas on each sample are reported. There is very little change in surface or interface quality at the six points so sampled on W32F. The data for W44F lie within the range of variation of the W32F data, so these two wafers appear to have equal quality. The other nonuniform wafer, W18F, is somewhat worse in interface and surface quality. Whether this difference in RBS quality is significant in terms of device yields remains to be seen. The two Westinghouse wafers, which have low-temperature epilayers intended to be of low crystallinity, clearly differ from the vendor wafers throughout the epilayer.

Figure 19 shows a RBS spectrum from W312F. The very high surface yield shows that there is little long-range order in the orientation of the surface material, and the interface scattering yield approaches the

Curve 739204-A

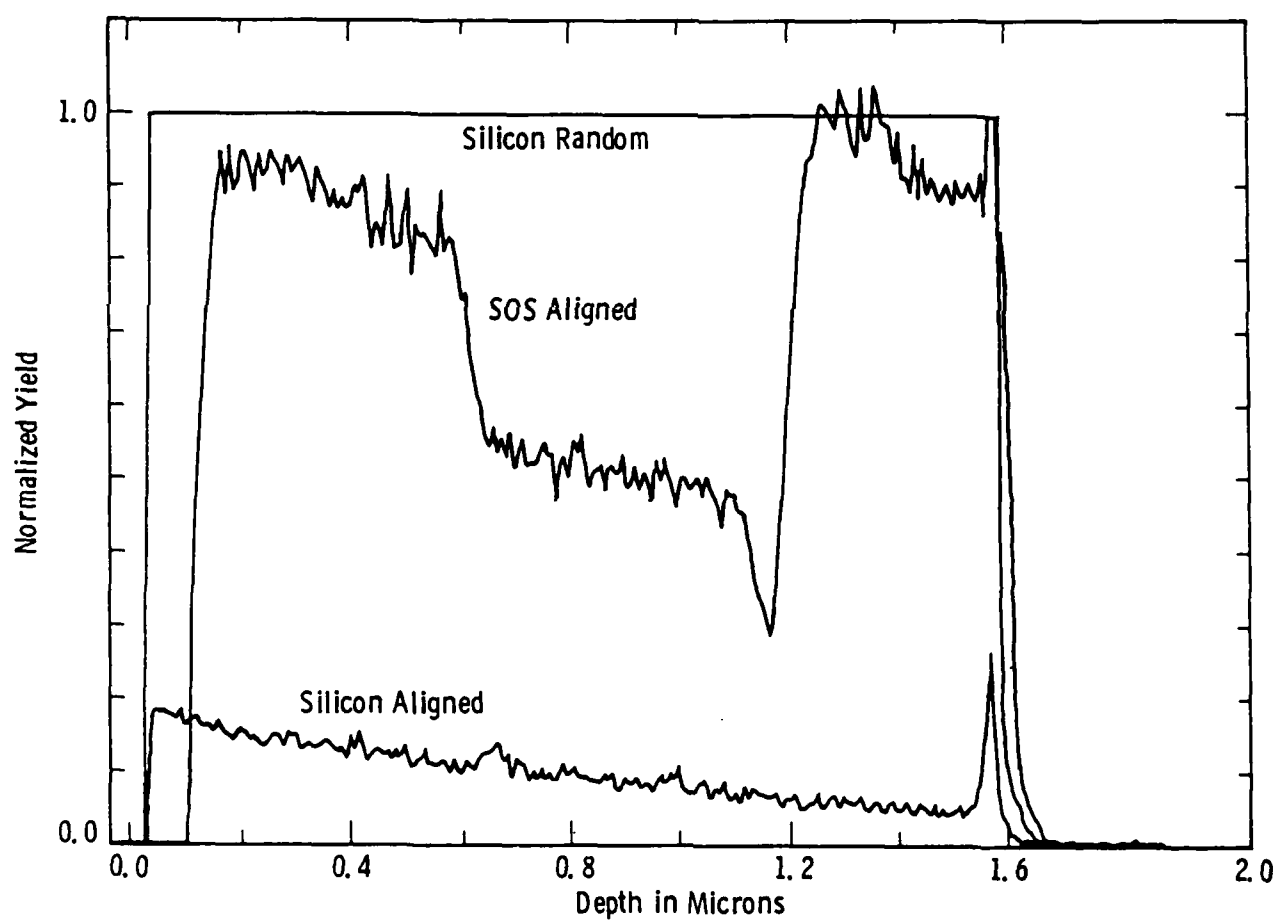


Figure 19. Rutherford backscattering spectrum from low-temperature epi wafer W312F.

random yield. The RBS technique cannot distinguish polycrystalline from amorphous material.

The RBS measurements were carried out by W. J. Choyke at the University of Pittsburgh High Energy Ion Beam Laboratory.

3. CHARACTERIZATION BY NEW METHODS

3.1 Raman Spectroscopic Measurement of Layer Stress

Raman spectroscopy has been used to measure the stress in silicon films grown epitaxially on sapphire substrates under diffused conditions. Silicon-on-sapphire wafers grown at both Westinghouse and Union Carbide have been evaluated by this technique.

A silicon film is compressed in its plane when grown epitaxially on sapphire.⁽¹⁸⁾ The strain in SOS is adequately explained by the difference in the thermal expansion coefficients of silicon and sapphire, that of sapphire being roughly twice that of silicon. At the growth temperature, 1000°C, it is assumed that the silicon is strain-free, but upon cooling, the thick sapphire substrate compresses the thin silicon film. For $\langle 100 \rangle$ silicon grown on the $\langle 10\bar{1}2 \rangle$ sapphire surface, the room-temperature lateral strain is -3×10^{-3} .⁽¹⁹⁾ This lateral strain induces a band structure change that is ultimately reflected in the various transport coefficients of the SOS film. In particular, electron Hall mobility is reduced to 50% of its bulk value.⁽²⁰⁾ The electron mobility also becomes slightly anisotropic in the $\langle 100 \rangle$ plane.⁽²¹⁾ Furthermore, part of the strain is relaxed by defect formation, which has detrimental effects on the carrier-scattering processes in the SOS film. It is therefore essential to include film stress measurements in a comprehensive evaluation of SOS wafers, and Raman scattering provides us with a sensitive, nondestructive method of doing so.

A photon of energy, $h\nu$, can interact with a set of oscillators which resonate at a lower frequency, ν_0 , to produce beat frequencies. In semiconductors there are always two sets of oscillators with which photons can interact -- the optical and acoustic modes of lattice

vibration. The interaction of photons with optical phonons is called Raman scattering. In the scattering process, the incident photon gives part of its energy, $h\nu_i$, to the lattice in the form of a phonon of energy, $h\nu_o$, and emerges with a lower energy, $h\nu_s$:

$$h\nu_s = h\nu_i - h\nu_o \quad (4)$$

This down-converted frequency shift is the Stokes-shifted scattering. If the lattice of the semiconductor is already in an excited state, the scattering process can result in the emission of a more energetic photon:

$$h\nu_s = h\nu_i + h\nu_o$$

These up-converted frequency shifts are the anti-Stokes-shifted scattering modes. Normally the intensity of the anti-Stokes modes is much weaker than that of the Stokes components because the probability for phonon absorption is lower than that for phonon emission by a factor of $\exp(h\nu_o/kT)$.

The Stokes Raman spectrum of unstressed silicon exhibits a single peak at $\nu_s = \nu_i - \nu_o$, where ν_o is the frequency of the triply degenerate optical phonons of zero crystal momentum ($q \approx 0$). When a uniaxial stress is applied, the Raman peak exhibits splittings and shifts which are linear in the applied stress. From the observed splittings of the Raman peak with applied stress along $\langle 100 \rangle$ and $\langle 111 \rangle$ directions, Anastassakis et al.⁽²²⁾ have obtained the first experimental values for the phenomenological coefficients which describe the changes in the spring constant of the $q \approx 0$ optical phonons with strain. The shift in the Raman peak energy thus provides a measurement of layer stress. The coefficient of stress has been reported as 2.49 kbar per wave number (cm^{-1}).^(14,23) Stress in SOS wafers has been measured using a polished silicon wafer as a reference standard. The dominant silicon peak, which appears at $\sim 520.5 \text{ cm}^{-1}$ for the silicon standard, is shifted toward higher frequencies for SOS wafers, indicating compressive stress.

3.1.1 Raman Method

We have used a Spectra Physics argon-ion laser in conjunction with a Spex double monochromator to obtain the Raman spectra of Union Carbide and Westinghouse SOS wafers. The experimental set-up is shown schematically in Figure 20. The Ar^+ laser beam ($\lambda = 514.5 \text{ nm}$) was focussed by means of a lens system onto the sample, which was placed face down in a sample holder. The sample holder was teflon coated, so that the samples did not touch metal or other sources of contamination, and had five access holes for the laser beam, one central and four peripheral holes. This allowed us to look at five different spots on the same wafer in order to determine whether the stress was uniform across the area on the film. The incident laser beam passed through a small hole in a 45° mirror, so that the backscattered light was reflected by the mirror into another lens which focussed the scattered light onto the entrance slits of the double monochromator, while the direct reflection from the wafer surface passed back through the hole in the 45° mirror. The second focussing lens was mounted on precision x-y-z translation stages in a stable and flexible configuration. A narrow-band filter was used to block a plasma line which otherwise tends to swamp the Raman signal for silicon at $\sim 520.5 \text{ cm}^{-1}$. The monochromator was freshly realigned before the experiments to improve the spectral resolution.

The system alignment was peaked up using a liquid carbon tetrachloride sample. The Raman spectrum for carbon tetrachloride is sharply defined and can be used to calibrate the spectrometer wavenumber readout gauge. A polished silicon wafer, used as the standard in these experiments, was then placed in the sample holder, and the system alignment was touched up to obtain the maximum signal-to-noise ratio at the Raman peak at $\sim 520.5 \text{ cm}^{-1}$.

The silicon standard had the same $\langle 100 \rangle$ orientation as the SOS wafers and had a damage-free surface finish so that the Raman spectrum of the standard represented stress-free silicon. The Raman spectra of

Dwg. 7762A21

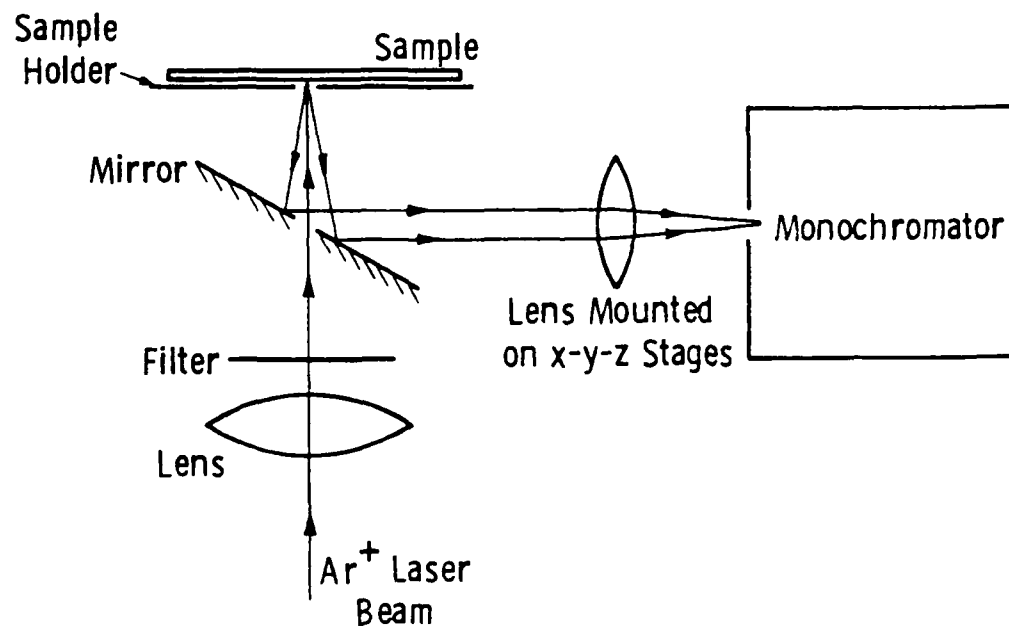


Figure 20. Schematic of experimental set-up for Raman scattering.

the SOS wafers exhibited a clear upward shift in peak frequency as compared with the silicon standard peak at $\sim 520.5 \text{ cm}^{-1}$, indicating compressive stress. An example of this is shown in Figure 21. The peak frequency of each sample was computed by bisecting the distance between the two half-maximum points. The full width at half maximum (FWHM) of each peak was calculated as well in order to estimate the crystal quality of the sample.

In the earliest runs we observed a drift in the calibration of the Raman spectrometer. This was mainly due to temperature changes in the laboratory. The calibration drift was large enough to obscure the stress-induced Raman shift in the early runs. We therefore developed a procedure to compensate for this drift. The silicon standard wafer was measured at the beginning and end of each run, and at frequent intervals during the run. The observed peak of the silicon wafer was used to derive a best-fit linear baseline. The baseline was then used to interpolate between the silicon standard measurements. All SOS data were compared to the baseline for calculations of stress-induced Raman shift.

The measured linewidths were fairly broad because of the wide monochromator slits (200-300 μm) used, reducing the system resolution to about 4 cm^{-1} , while also greatly reducing the time required to record a spectrum, and increasing the signal-to-noise ratio. A study was carried out, using an SOS wafer and the silicon standard, to determine the effect of narrowing the slits down on the spectral resolution. The results are plotted in Figure 22. The linewidth is directly proportional to the slit width, and the slope of the plot is equal to that of the quoted spectrometer bandpass plotted as a function of the slit width, also displayed in Figure 22.

The precision of our technique was determined by a set of repeated measurements on the silicon standard wafer. The average linewidth (FWHM) is 6.4 cm^{-1} , which does not represent the true Raman linewidth, as noted in the paragraph above. In this series of nine

Curve 732255-A

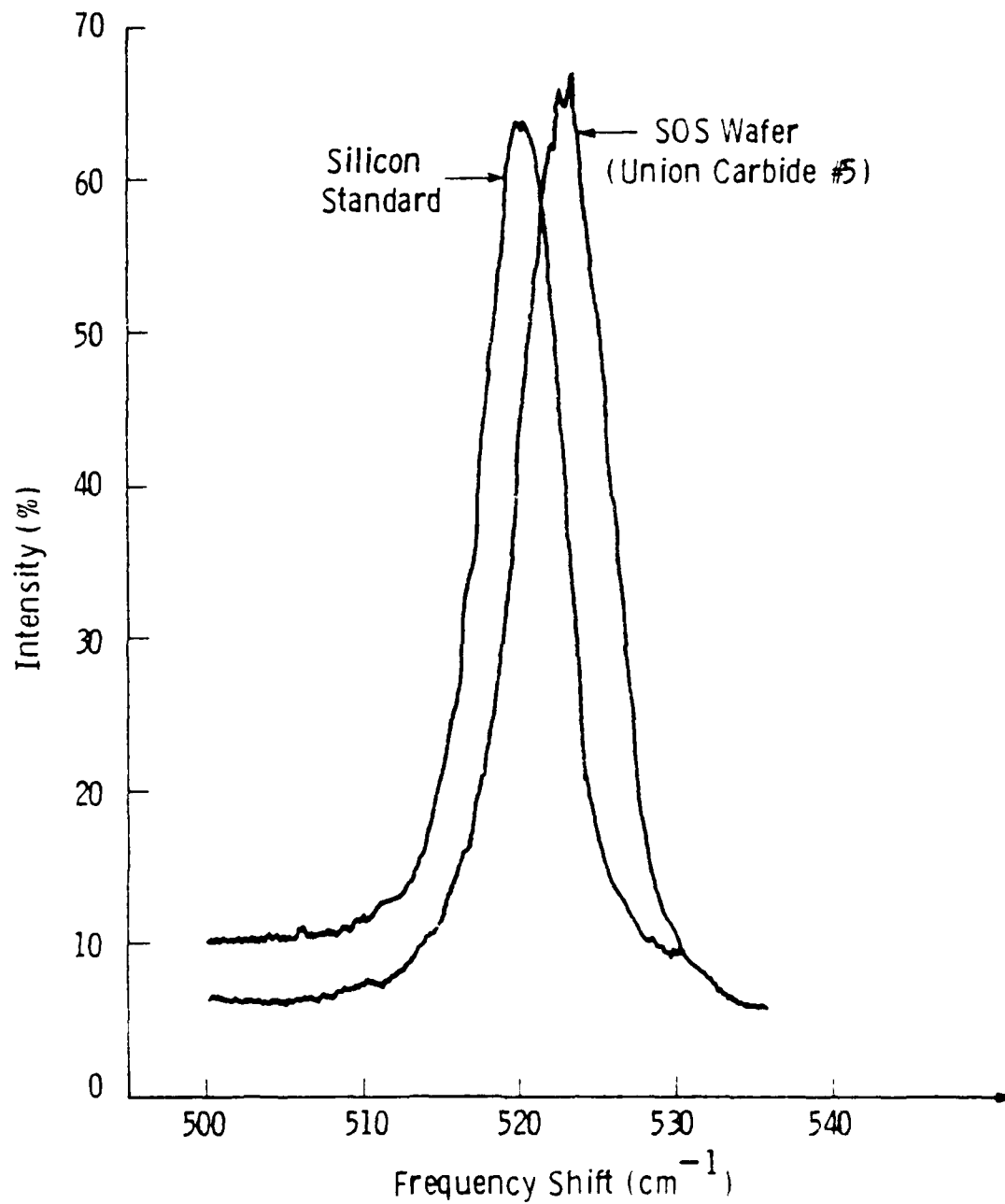


Figure 21. Raman spectra of SOS and bulk silicon wafers.

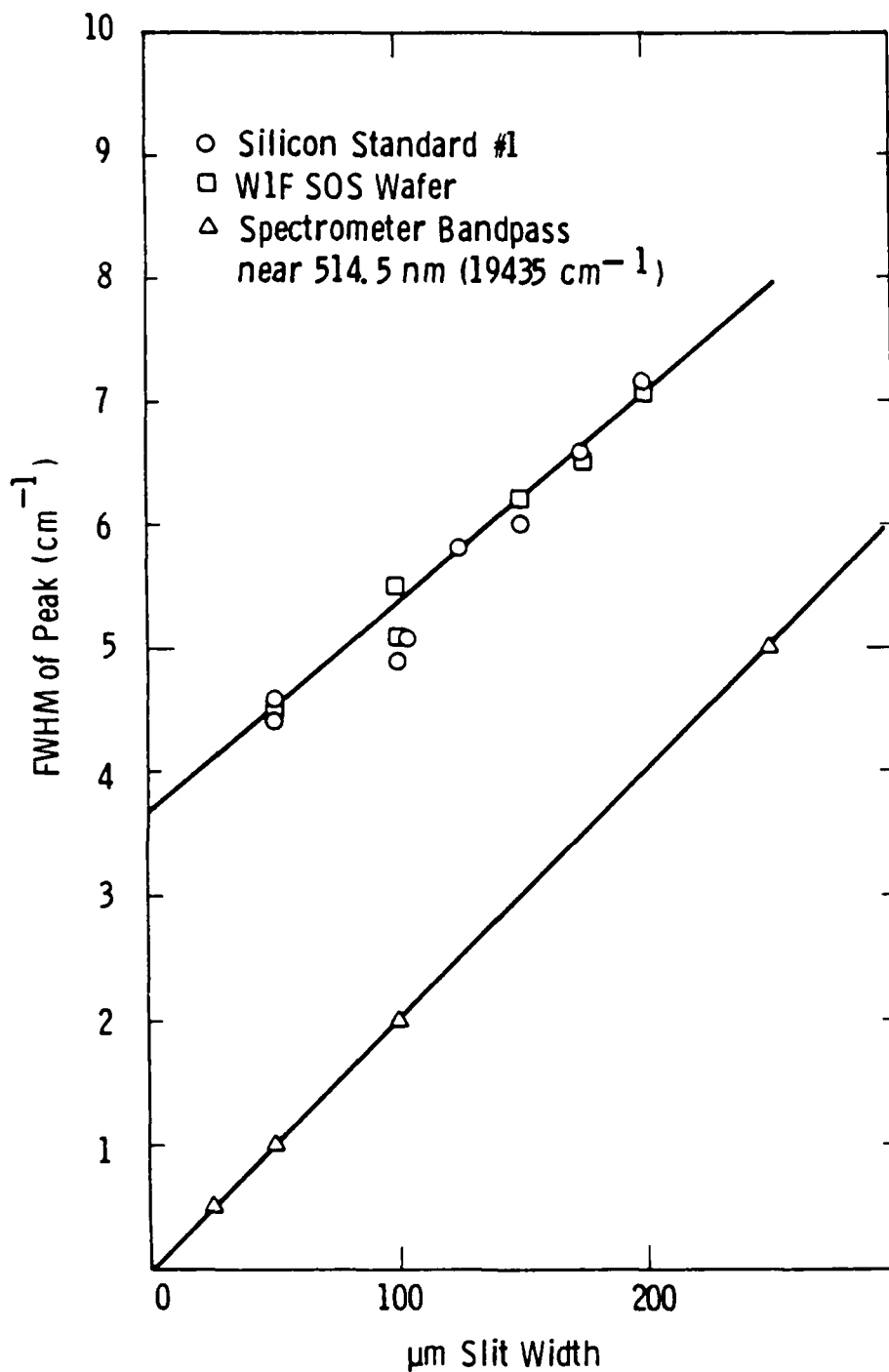


Figure 22. Comparison of SOS wafer and silicon standard to determine effect of narrowing the slits down on the spectral resolution.

repeated measurements, the rms variation in the peak frequency was 0.42 cm^{-1} . This corresponded to an uncertainty of 1.05 kbar in layer stress and was the least increment of stress that we were able to resolve with our technique.

3.1.2 Raman Layer Stress Data

Raman spectra were taken for the vendor wafers and Westinghouse grown epilayers with the instrument settings and baseline correction described in the preceding section.

Figure 23 shows the Raman peak shift data for the vendor wafers. The average peak shift is 3.09 cm^{-1} , and the rms variation about the mean is 0.44 cm^{-1} , as shown in Table 5. The Westinghouse epilayers grown at normal temperatures (970 and 1000°C) gave rise to the Raman peak shift distribution shown in Figure 24. There were 21 wafers in this data set, with a mean peak shift of 3.09 cm^{-1} and rms variation of 0.47 cm^{-1} . Figure 25 shows the peak shift data for the Westinghouse low-temperature epilayers (880 and 900°C), where the mean value is significantly lower at 1.91 cm^{-1} .

The Raman linewidth data are shown in Figure 26, where the linewidth of each wafer is plotted for three groups of wafers. All of the wafers in group 1 were vendor wafers, group 2 comprised the Westinghouse low-temperature epilayers, and group 3 represented measurement and remeasurement of silicon wafers. The linewidth of the low-temperature epi wafers is significantly larger than that of the vendor wafers and the silicon standards.

Much of the variation in peak shift and linewidth comes from imprecision in the measuring technique. Figure 27 shows the distribution of data from simply remeasuring a silicon wafer repeatedly during SOS wafer runs. The baseline correction was applied to derive a calibration which is linear with time for each run. The silicon wafer remeasurements are compared to the computed baseline value in obtaining the distribution shown in Figure 27. This method will compensate for

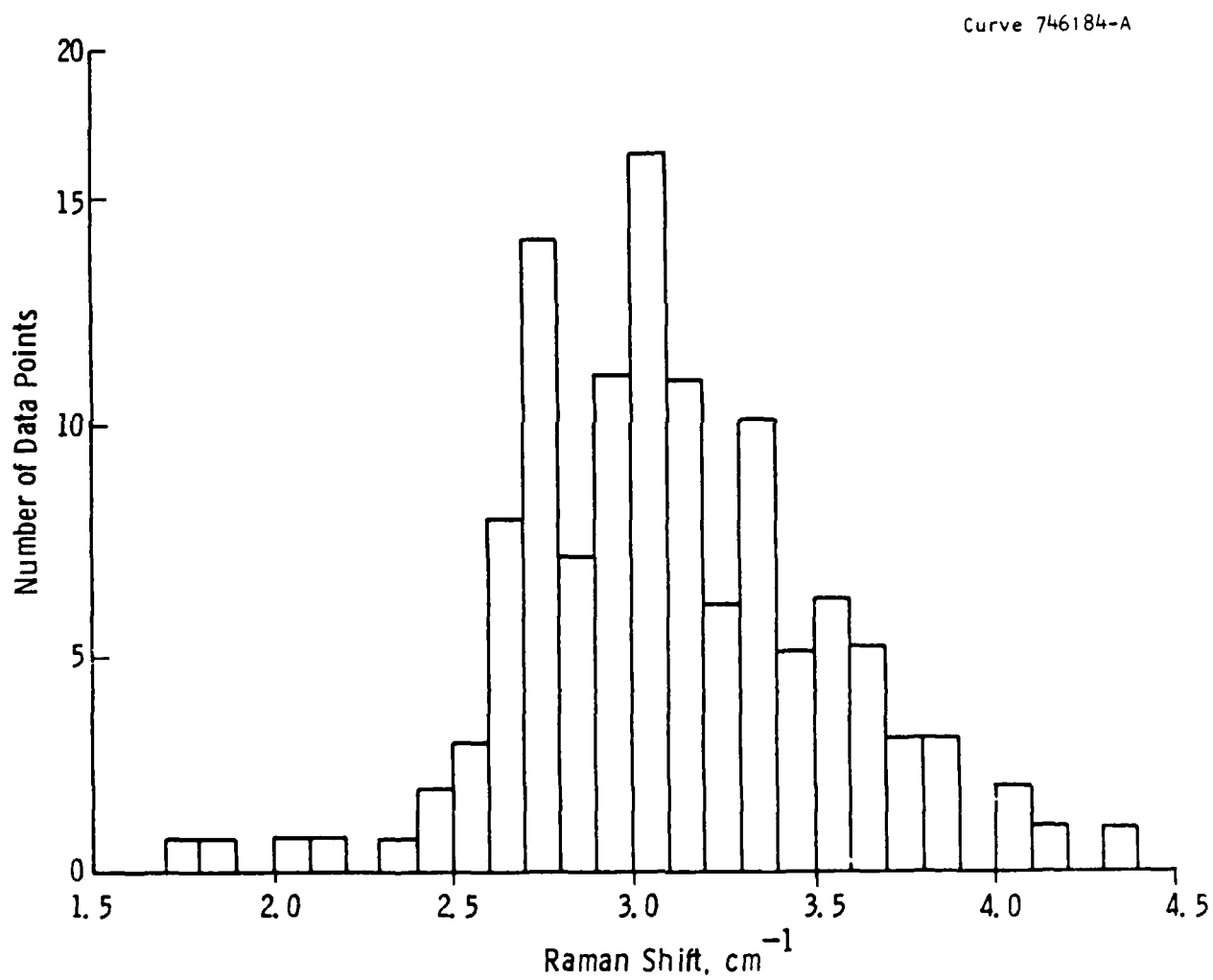


Figure 23. Distribution of Raman shift data for vendor wafers.

Table 5
Summary of Raman Results for SOS Wafers

Average Layer Stress kbar	Number of Data Points	Raman Peak Shift				Peak Width	
		Average cm ⁻¹	Low cm ⁻¹	High cm ⁻¹	rms cm ⁻¹	Average cm ⁻¹	rms cm ⁻¹
Vendor Wafers	119	3.09	1.76	4.34	0.44	6.54	0.39
Westinghouse Normal-Temperature Epilayers (T = 970, 1000°C)	21	3.09	2.08	4.04	0.47	7.13	0.98
Westinghouse Low-Temperature Epilayer (T = 880, 900°C)	12	1.91	1.12	2.63	0.53	9.08	0.43
Solid-Phase Epitaxial Regrown SOS	2	2.28	2.25	2.30	-	6.7	-
Silicon Standard Wafers and Remeasures	54	0	-1.81	1.44	0.42	6.38	0.59

For Stress Level σ (kbar) and Raman Peak Shift σ (cm⁻¹), we have $\sigma = 2.49 \times \delta$

Conversion to other units:

$$1 \text{ kbar} = 10^9 \text{ dyne/cm}^2 = 10^8 \text{ Pa} = 1.45 \times 10^4 \text{ psi}$$

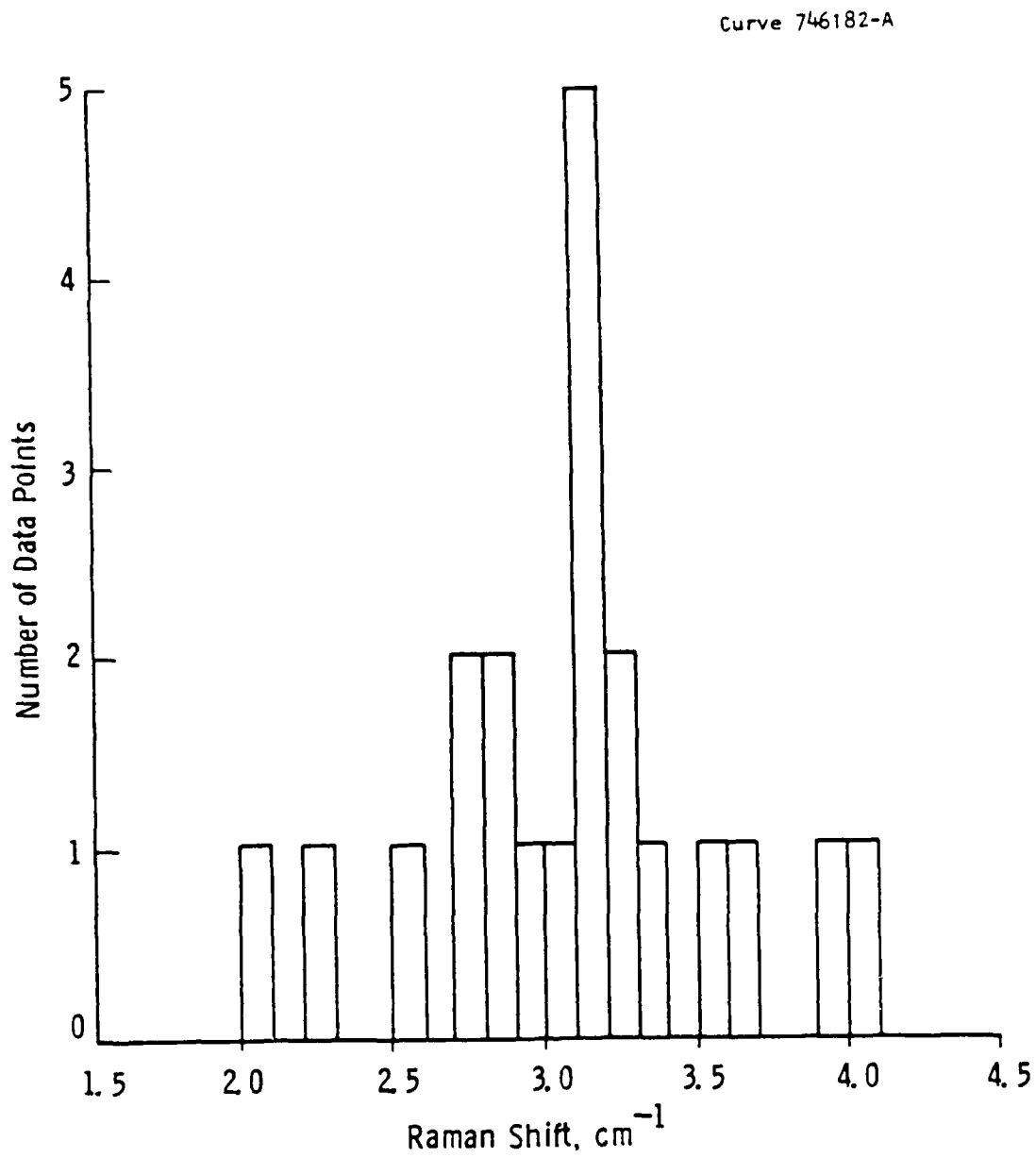


Figure 24. Distribution of Raman data for Westinghouse wafers excluding low-temperature epi.

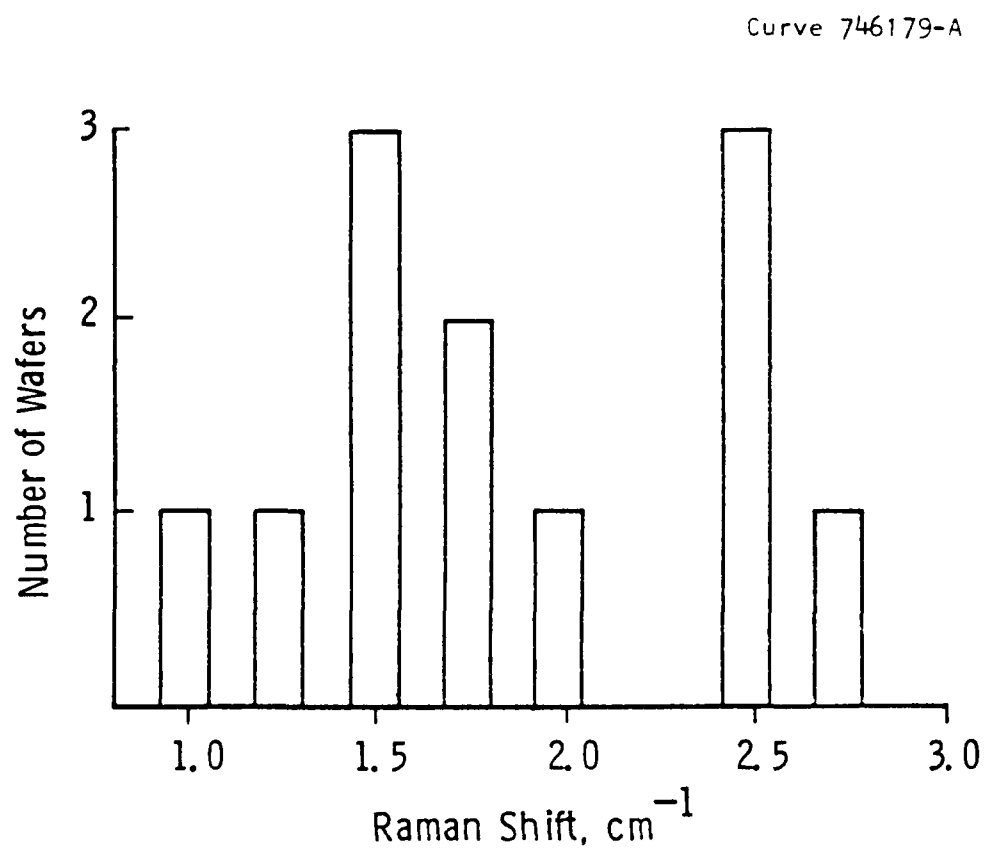


Figure 25. Distribution of Raman data for low-temperature epi wafers.

Curve 732253-A

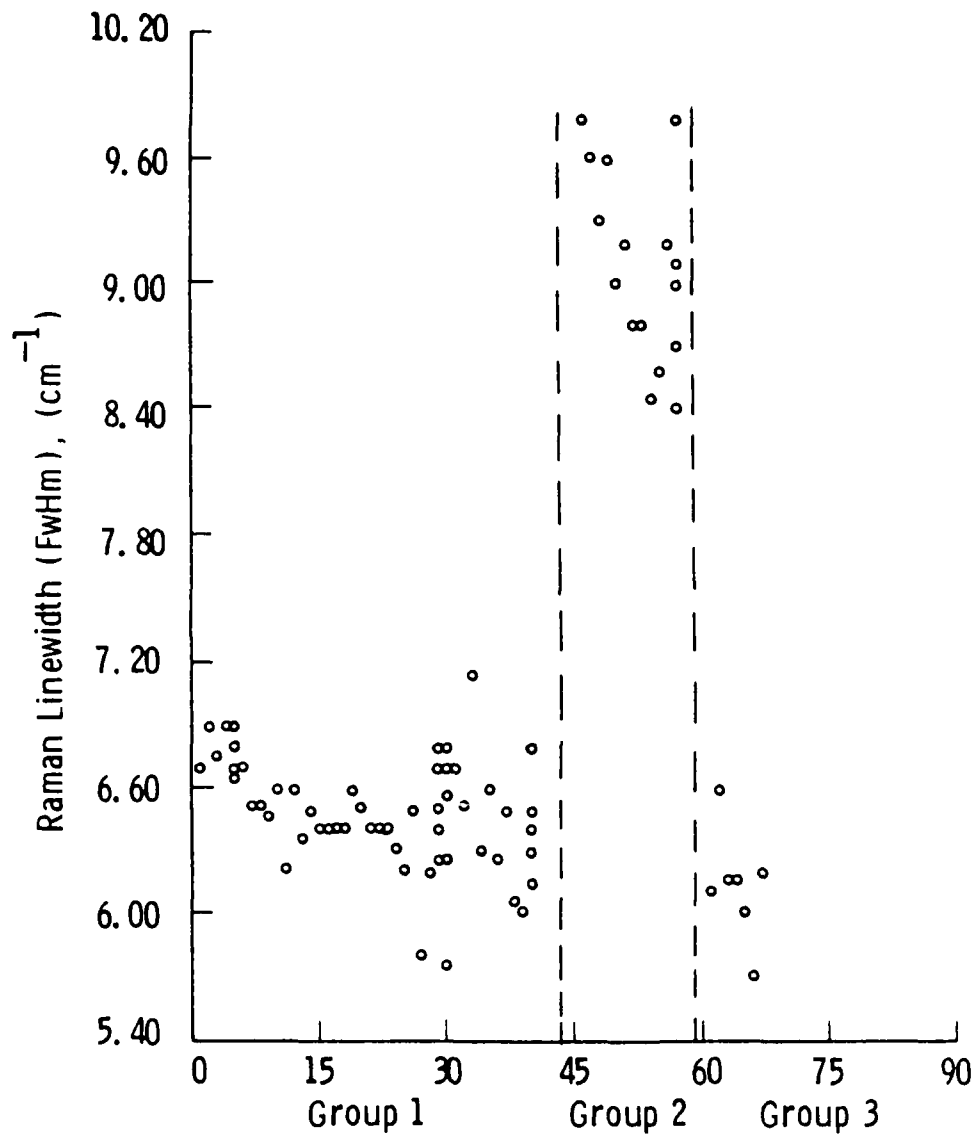


Figure 26. Raman linewidth for three groups of wafers: group 1, vendor wafers; group 2, low-temperature epi wafers; group 3, silicon wafers.

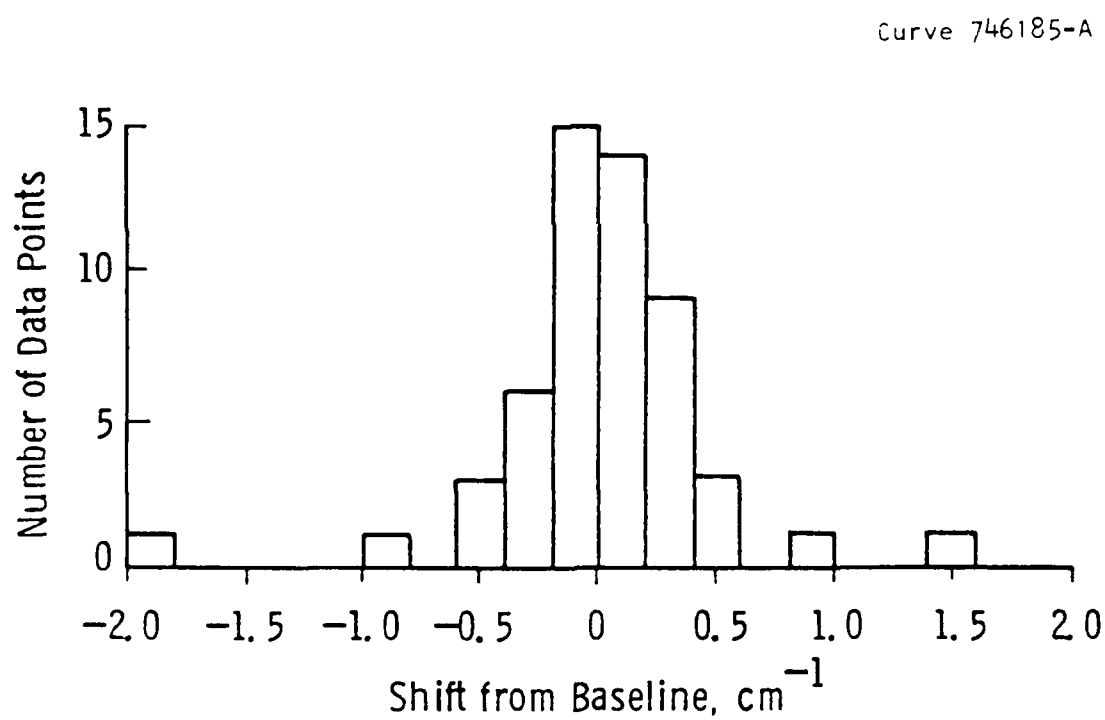


Figure 27. Distribution of Raman data from silicon wafers.

drift in the calibration of the monochromator due to changes in room temperature. The magnitude of the rms variation in remeasures of the silicon standard is 0.42 cm^{-1} (see Table 5). This is almost the same as the rms variation for the vendor wafers and the high-temperature epilayers. We conclude that the width of the distribution shown in Figures 23 and 24 is due mainly to this source. Both groups have the same mean value, so the layer stress is about 7.7 kbar for the Union Carbide SOS wafers and the SOS epilayers grown at Westinghouse at high temperatures ($T = 970, 1000^\circ\text{C}$).

The layer stress is significantly different in the epilayers grown at low temperatures. The difference in the mean values is 1.18 cm^{-1} , which exceeds the sum of the standard deviations ($.97 \text{ cm}^{-1}$) of the two groups. The linewidth of this group is also significantly higher, as shown in Figure 26 and in Table 5.

3.2 Ultraviolet Scattering Haze Measurement

3.2.1 Introduction

The measurement of Ultra-Violet Scattering (UVS) haze was proposed as a topic for study in order to meet the requirement for a rapid, simple, nondestructive inspection method for evaluation of SOS starting material. The selection of this method was based on the accepted practice of optical inspection as a screening test for SOS wafer lots. SOS wafers were held in a bright white light and inspected from several viewing angles. The appearance of the epilayer surface was classified as clear or cloudy in various degrees according to the judgement of the inspector. This technique has been widely used among suppliers and users of SOS wafers, and has been shown as a dependable method of predicting eventual device yield and performance.⁽²⁾ However, this method is qualitative and difficult to standardize. Classification of wafers as clear, slightly hazy, or very hazy depends on a judgement by the inspector. The implementation of this technique could be

improved by finding a quantitative, nonsubjective method to measure the haziness of the epilayer surface.

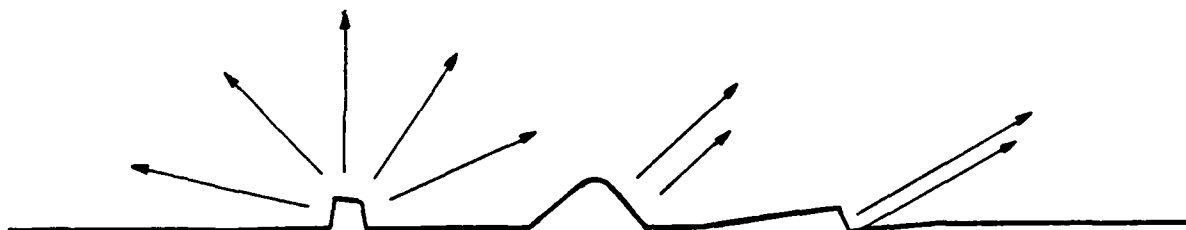
The visual inspection method is based on observation of scattered light from the epilayer surface. The distinctively cloudy appearance of a poor-quality epilayer is easily distinguishable from the clear surface of a good silicon wafer, especially when viewed at an oblique angle with respect to the illumination. The method selected for study directly measures the amount of light scattered at an angle some distance away from a direct equivalent to the visual inspection, but quantitative and capable of calibration. Because of this relationship to an accepted technique, the scattering haze measurement method was considered a relatively low-risk approach to SOS wafer evaluation and highly likely to result in a dependable screening method for SOS starting material.

Scattering from a nominally planar surface can arise from two causes (see Figure 28). Deviations from a perfectly plane surface will cause scattering due to local variations in the specular reflection angle. Also, surface asperities can cause scattering through large angles by diffraction effects if the dimensions of the asperities are small. The amount and distribution of scattered light will thus depend on the texture of the epilayer surface. Scattering may also arise from local inhomogeneities in the material, as might arise from crystal defects. Local changes in material quality will cause variations in the amplitude and phase of reflected light, resulting in amplitude and phase of reflected light, resulting in scattering. Detailed measurements of scattering may allow the identification of the cause, and further characterization of the epilayer for the size, shape, and distribution of surface features or material inhomogeneities.

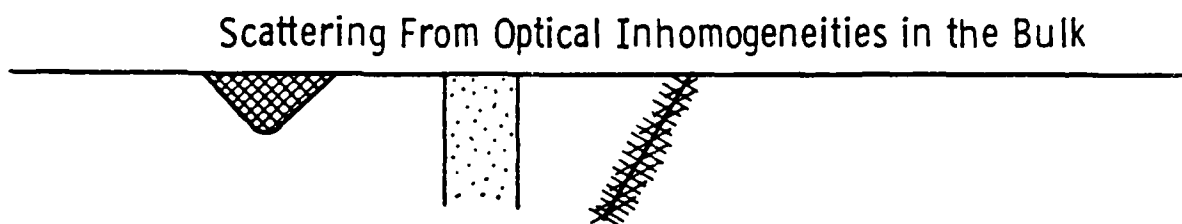
3.2.2 Ultraviolet Scattering Method

The Ultraviolet Scattering (UVS) haze method depends on the detection and measurement of the low levels of light scattered at some

Dwg. 9358A50



Scattering From Surface Asperities



Scattering From Optical Inhomogeneities in the Bulk

Figure 28. Sources of Haze

angle away from the direct specular reflection of the light incident on the wafer surface. Care must be taken to avoid spurious signals introduced by stray light that may not even strike the sample under test. The apparatus diagrammed in Figure 29 has been found to be satisfactory. The light from an optical source is collimated by a lens and directed toward the wafer being characterized. Both mercury arc lamps and helium-cadmium lasers have been used as optical sources. The incident beam is collimated for better control of stray light paths and for a well-defined geometry of angle of incidence and angle of scattering. The direct specular reflection from the sample surface returns along the path of the incident beam. Experiments have been tried with non-normal incidence angles, but no advantage was discovered in such an arrangement. Stray light from the reflected beam, from uncollimated elements of the source, and from first-surface reflections at the lens are trapped in a flat-black painted baffle box. The baffle is a series of parallel aluminum plates spaced about two inches apart, with circular apertures large enough to pass the incident beam. The plates are enclosed on all sides by aluminum covers. The purpose of the baffle is to prevent reflection of stray light from a nonabsorbing surface, especially reflections at glancing angles of incidence.

The detector is held at a selected angle at some distance from the sample. Another lens is used to collect the light scattered at the selected angle and focus it on the detector aperture. The lens focal length of 500 mm determines the spacing between sample and detector. The collecting lens is not necessary but does give an increased signal, which is helpful when using the laser as an optical source. Another baffle box is used between the sample and detector to suppress stray light paths.

The wavelength of the scattered light is an important consideration. Wavelengths longer than about 440 nm will penetrate the silicon epilayer well enough to give significant scattering from the back surface of the wafer. The back surface is lapped and is a very strong scattering source. The wavelength must be chosen so that no appreciable

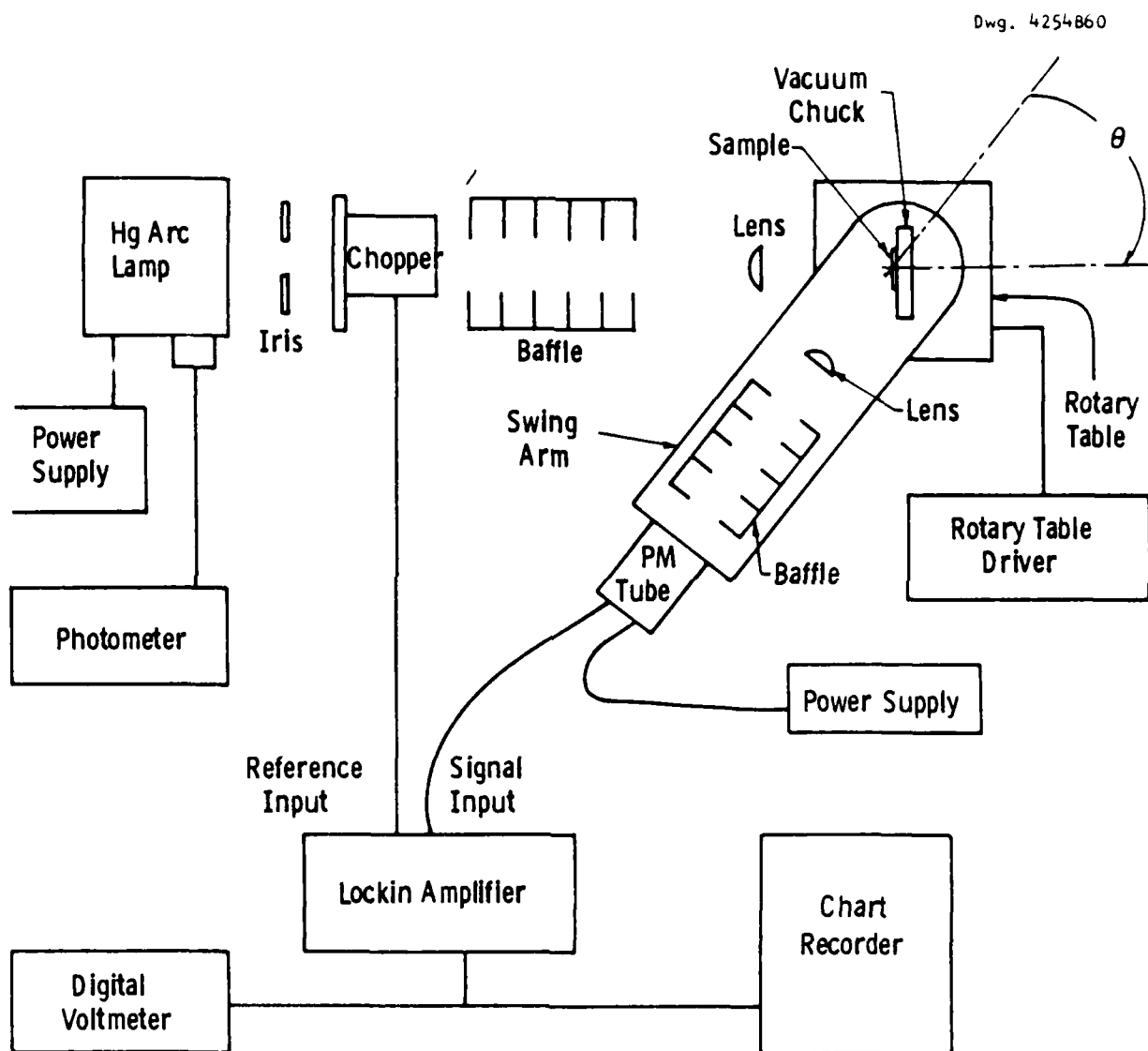


Figure 29. Apparatus for measurement of UV scattering haze.

signal originates from the back surface. This condition is well satisfied by using a helium-cadmium laser with the appropriate mirrors to select the 325 nm laser line. The mercury arc lamp is a broad band source and the wavelength restriction must be external to the lamp. We have used a solar-blind photomultiplier tube to provide the required wavelength discrimination. Such detectors are sensitive only in the UV, with a spectral response curve that begins to roll off at 300 nm and becomes negligible beyond 400 nm. Because of the characteristic of the detector, long-wavelength light scattered from the back of the wafer does not result in an electrical signal.

The incident light is modulated by a chopper wheel located immediately next to the source. The signal from the detector goes to a lock-in amplifier which is phase locked to the chopper wheel. This phase-sensitive detection scheme is the conventional method for discriminating against nonsynchronous light inputs such as room light, and for moving to a less noisy frequency range in the response of the photomultiplier tube.

Two different angular scan procedures have been used. In the first procedure the detector, baffle, and collecting lens are mounted on a movable arm. The arm rotates about a center at the sample by means of a rotary table driven by a stepping motor through a reduction gear. The scattering angle, θ , defined as the angle between the axis of the incident beam and the axis of the detector arm, can vary from about 10° to more than 90° . In the second configuration, the detector is placed at fixed scattering angle of 30° , and the sample is rotated through an angle θ about an axis normal to its surface.

For both types of angular scans, the sample wafer is mounted in a vertical plane and held fast by a vacuum fixture. The detector moves in a horizontal plane for scans of the scattering angle θ . By convention, the wafers were mounted in the vacuum chuck with the flat at the top of the wafer. When the sample rotation angle θ was being scanned, the sample was mounted so that it rested on the flat at the

bottom of the wafer. The vacuum fixture was aligned with a spirit level to provide a reliable zero angle for θ . Scans of θ always took place in the clockwise direction when viewing the epilayer surface. Because the rotary table does not have an angular position signal output, it is necessary to synchronize the θ scan with the chart display. At the beginning of a scan, the rotary table scan and the chart time base are started simultaneously. The angular position is monitored by watching the digital readout on the rotary table driver chassis. When the θ scan reaches the preset index value of 360° , the rotary table stops and the operator causes the chart recorder to make a mark on the scan record. Experience has shown that the precision of this calibration procedure is more than adequate, being repeatable to about ± 2 degrees in a 360° rotation.

To avoid possible scattering from the sample holder, the incident beam is restricted to illuminate a spot at the center of the sample of about 25 to 30 mm diameter. This also eliminates scattering from any defects or handling marks at the edge of the wafer.

Some data were taken with the wavelength restricted to 200, 280, or 400 nm. The wavelength was selected by a narrow-band interference filter placed at the aperture of the detector. The time constant of the response of the lock-in amplifier was set at 1 second for good noise suppression. This resulted in a slight shift of about 3° in the rotation angular scans where the scan rate was $3^\circ/\text{sec}$. There were no features observed in any of the SOS wafer scans for which the time constant limited the resolution.

3.2.3 UVS Haze: Scattering Angle Scans

The amount of light scattered from a surface depends on the amplitude of surface roughness and the degree of inhomogeneity of the material optical properties. In addition, the angular distribution of the scattered light depends on the detailed texture of the surface.⁽²⁴⁾ Inferences can be made about the surface texture based on

the measured scattering amplitude in scattering angle scans. The angular dependence is also of use in selecting an optimum angle for haze measurements. Finally, angular scans have proved to be useful in detecting spurious signals from stray light paths, and in identifying and eliminating the spurious signals.

The technique is described in the preceding section on UVS method. The scattering angle typically ranged from 10° to about 55° . The results are shown in Figure 30 for several different samples. A mechanically lapped silicon wafer gave the highest scattering signal at all angles, followed by two SOS wafers grown at Westinghouse at sub-optimal deposition temperatures. The vendor SOS wafer and the polished silicon wafer were the lowest scattering sources. These data were taken with the helium-cadmium laser as the optical source. The power available from the laser is about 2 mW. A similar scan taken with the mercury arc lamp optical source is shown in Figure 31. Here the topmost curve originates from a silicon wafer roughened by a chemical etching procedure. Etch pits and facets are visible on the surface of the wafer when it is viewed in a low-power microscope. The increased brightness of scattering at the intermediate angle can also be seen by human eye.

A comparison of data from SOS and polished silicon wafers reveals little structure as the scattering angle varies. None of the SOS or polished silicon wafers show peaks such as that observed with the etched silicon wafer. The shapes of all of the SOS curves are very similar and no two curves ever cross. We concluded that there is no significant variation in the surface texture that can be detected by scattering angle scans. All of the SOS wafers appear to be similar in this respect in the θ scans. The amplitude of the surface texture does, of course, give an observable change in scattering level and can be measured at a fixed scattering angle.

Comparing the scattering from two SOS wafers, we find that the ratio of the scattered light signals is approximately constant as the scattering angle θ varies. This verifies that the SOS curves are

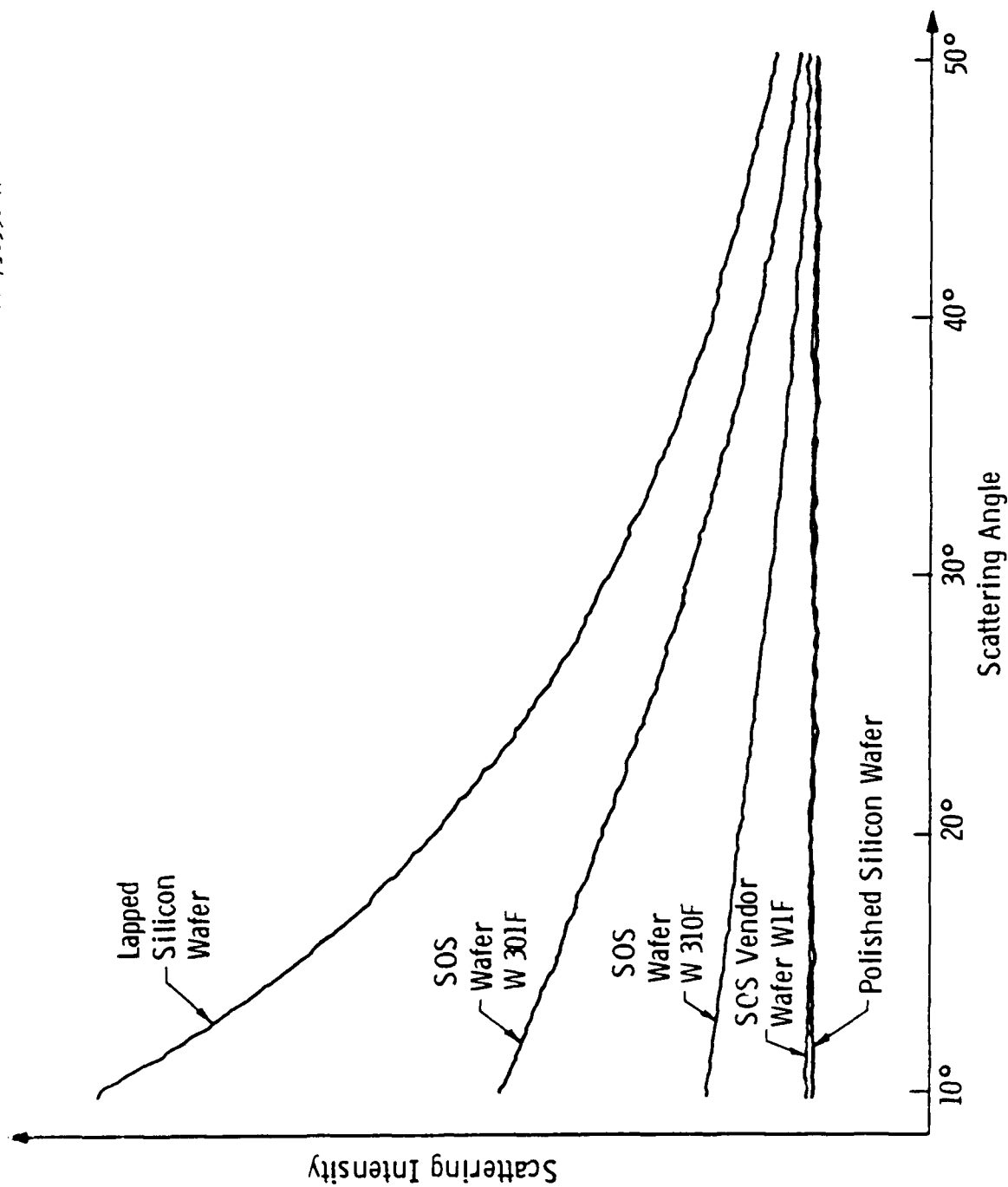


Figure 30. Intensity of scattered UV light versus scattering angle θ .

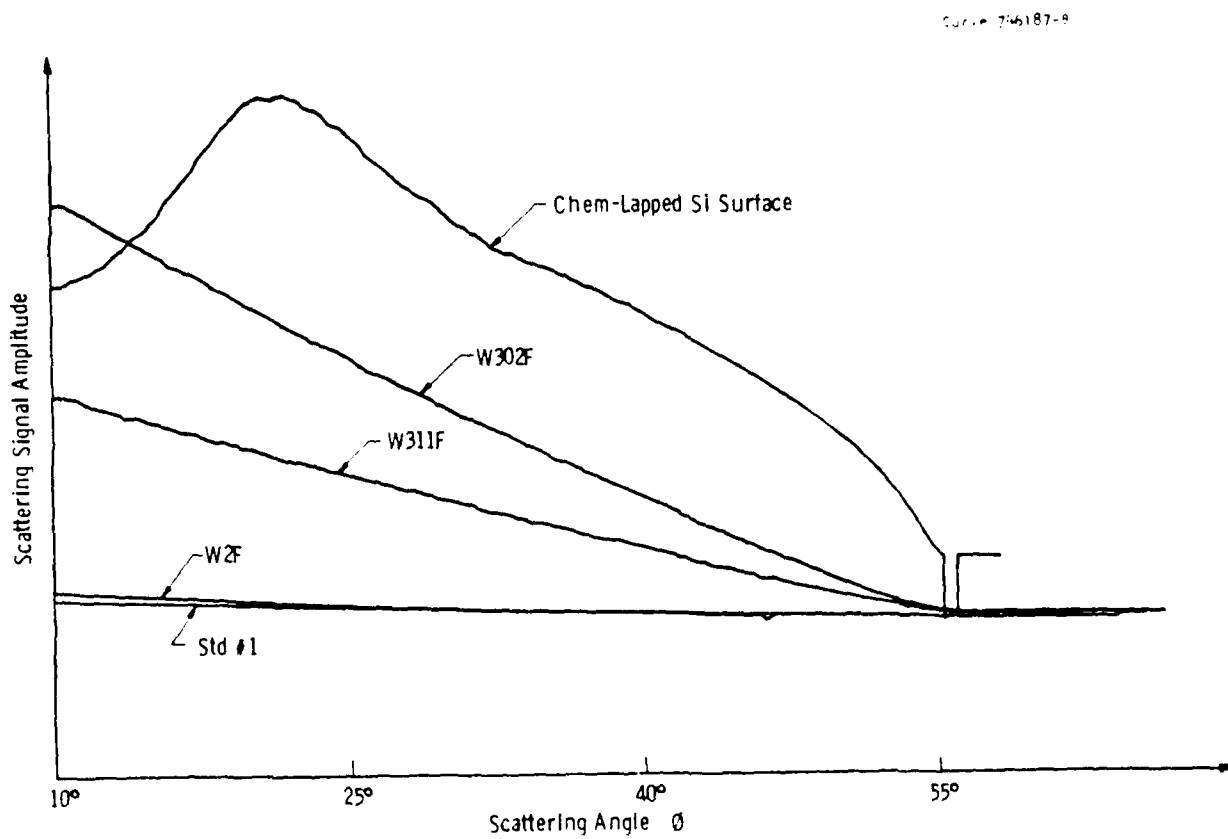


Figure 31. Scan taken with mercury arc lamp optical source.

similar and shows there is no preferred angle at which to measure haze. The fixed angle for haze measurements was chosen to be about 15° in order to take advantage of the greater signal available at smaller scattering angles.

3.2.4 UVS Haze Measurements

3.2.4.1 UVS Haze Method

The measurements of SOS wafer haze were made with the equipment described in Section 3.2.2, "Ultraviolet Scattering Method." The mercury arc lamp was used as the optical source. Apertures were used to restrict the illuminated area on the wafer under test to a spot 25 to 30 mm in diameter at the center of the wafer. Changing the spot size did not change the haze number. The detector was a solar blind photomultiplier tube which restricts the observation of scattered light to wavelengths shorter than 350 nm. The detector was fixed in position at a scattering angle of 15° . This angle is not critical and was chosen to take advantage of the larger signal available at smaller scattering angles. The wafers were held by a vacuum fixture in a vertical plane, perpendicular to the incident beam from the lamp. By convention, the wafers were mounted with the flat at the top of the wafer. The orientation of the wafer is important, as a rotation of a few degrees will measurably change the scattering signal. This effect is documented in Section 3.2.5, "UVS Rotational Scans." The importance of angular orientation was not understood at the time the haze measurements were made. The estimated accuracy of orienting the wafer flat was $\pm 10^\circ$ from horizontal. This amount of angular misorientation undoubtedly contributes some scatter to the haze data.

To discriminate against changes in the measurement calibration due to variations in lamp intensity and detector sensitivity, a standardization procedure was developed. The ideal standard would be a sample that could be inserted in place of a wafer to give a repeatable scattering signal. The amplitude of the scattering should be

approximately the same as that from an SOS wafer to avoid scale changes which would require further calibrations. The following samples were evaluated as standards: polished silicon wafers, lapped silicon wafers, chemically etched silicon wafers, lapped metal discs, ground glass discs, and sapphire substrates. These were not acceptable standards because the scattering was orders of magnitude different from an SOS wafer, or because the scattering signal was not repeatable upon removing and replacing the sample. Rather than attempting to fabricate a standard, one of the SOS wafers was selected to serve as a reference for comparison. The standard wafer was designated W1F. Experiments showed that the scattering signal from this wafer was consistently repeatable upon removing and replacing the wafer. Later measurements showed that this wafer had an unusually low variation of scattering versus rotation angle. Wafer W1F was remeasured at the beginning of each haze run and at frequent intervals during the run. The magnitude of the scattering signal from wafer W1F was assigned a baseline value of 100. Changes in the system calibration between runs were compensated by the remeasurements of W1F. Drift of the calibration during a single run was compensated by linear interpolation between repeated readings of W1F. As a result, all haze numbers are expressed as ratios of the scattering signal from each SOS wafer compared to W1F. This procedure is adequate for relative characterization of the haze observed in the wafers available for testing.

3.2.4.2 EWS Qualification Data

In this section we present data related to the reliability of the measurement technique.

The reliability of repeated measurements of the standard wafer W1F is a key to the consistency of the haze measurements. The data from repeated measurements of W1F during a single run were subjected to linear regression analysis. Readings on W1F were taken at the beginning of the run, at the end, and at approximately equal time intervals during the run. The independent variable is the time of measurements and the

dependent variable is the measured scattering signal. A linear fit to the data showed a 10.2% reduction in the signal during the run. Independent measurements of the intensity of the mercury arc lamp showed a 5.6% reduction during the run. This accounts for part of the drift observed in the standard wafer readings. The remaining 4.6% variation could be due to a drift in the sensitivity of the photomultiplier tube, or a change in the spectral output intensity of the lamp which would affect the intensity monitor and the photomultiplier tube differently. We did not attempt to measure either of these effects, although our experience showed that the photomultiplier tube was not very stable. After the linear drift of 10.2% is subtracted, there remains a residual variation of 2.8% runs in the repeated readings of WIF. This is attributed to random variations in the orientation and position in removing and replacement of the wafer that affect the amount of scattered light directed toward the detector. This residual variation also includes the effects of the detection system noise level. Similar results were obtained in analysis of a second run. The residual variation in standard measurements places a limit of $\pm 3\%$ on the precision of the technique as it is presently implemented.

The long-term repeatability of the haze measurement was assessed by compiling data on repeated measurements on selected wafers over time intervals ranging from a few minutes to several months. Any change in the scattering from the standard wafer should show up as a systematic drift of the haze numbers as a function of time. No such drift has been observed. Alteration of the standard wafer due to handling or contamination would also show up as a systematic change in haze numbers, since the wafers selected for comparison were subjected to much less exposure and handling than the standard wafer. Again, no effect of this kind is seen. The repeatability data are tabulated in Table 6. It can be seen that the rms variation in the normalized haze number is typically 5% or less. Wafers 9 and 22, which show larger variations, also have unusually high variations of scattering with respect to rotation angle.

Table 6

Repeatability Data with the Average Reading and rms Variation

WAFER NUMBER	READINGS												AVG	RMS
1	109	119	105	120	114	105	109	115	105	120	118	129	114.2	7.3
2	95	94	95	95	94	91	93	94	92	95			93.8	1.9
4	124	125	126	128	128	123	122	123	128	128			125.7	2.2
5	122	121	139	139	138	123	137						124.1	5.6
6	129	127	130										128.3	1.3
7	124	125	129										126.0	3.2
8	143	158	145										141.7	3.9
9	140	148	149										159.0	8.4
10	77	75											76.0	1.0
11	115	116											115.5	0.5
12	115	114											115.5	0.5
13	104	127											131.5	5.5
14	94	101											98.5	2.6
15	114	119											116.5	2.5
16	119	119											119.0	0.0
17	119	118											118.5	0.5
18	114	113											113.5	0.5
20	129	129											129.5	0.5
21	146	153											149.5	3.5
22	111	174											142.5	31.5
23	74	75											74.5	0.5
24	115	116											115.5	0.5
25	159												159.0	0.0

Part of the observed variation may be due to misorientation of the wafers during the repeated measurements.

The sensitivity of haze measurement to surface condition was also tested in qualitative ways. A few dust particles on the wafer surface did not change the measured haze. Cleaning the surface by blowing dust with dry nitrogen or Freon did not have an effect, except when liquid Freon was blasted onto the surface and a visible scum was deposited. Moderate wiping with lens tissue had no effect, but scrubbing sufficient to leave visible marks definitely increased the measured haze. Etching the surface with a selective etch also increased the haze. Growth of a thin oxide changed the haze only slightly.

These results show that this method gives a reliable, repeatable indication of the surface haze of SOS wafers. The measured haze is characteristic of the silicon epilayer and does not depend strongly on cleanliness or conditioning of the surface.

3.2.4.3 UVS Haze Measurement Data

The UV scattering haze was measured on each of the wafers purchased from Union Carbide. The only exceptions were wafers 18 and 44, which had been cut to make RBS samples, and wafers 32 and 58, which were etched as calibration samples for the epilayer thickness measurements. The haze values for the remaining 106 wafers are given in Table 7. The distribution of the haze numbers is shown in Figure 32. The distribution is relatively even about the mean value of 124.4 except for a few wafers with haze greater than 160. Twenty-six wafers had haze numbers less than the standard wafer (WLF set equal to 100 as the standard). Haze numbers ranged from 202 to 72, with rms variation about the mean of 29.1.

The other SOS wafers were measured in similar fashion. Table 8 presents a summary of the haze data for all SOS wafers studied in this program. The 106 Union Carbide 2-inch wafers are entered as item 1. Items 2-8 are wafers prepared at Westinghouse for this program. Items 9 and 10 are 4-inch SOS wafers recently purchased from two vendors for preliminary quality evaluation. Item 11 comprises the readings taken on polished silicon wafers, which served as the standard for an optically smooth surface.

Examination of Table 8 shows that all of the epilayers grown at Westinghouse are much hazier than the vendor wafers. For the low-temperature runs, items 2, 3, and 4, it was intended that the epi quality should be low. This was confirmed by the RBS and Raman linewidth studies. The run at 880°C showed the higher haze and also the greatest range of haze readings. The two runs at 900°C had lower standard deviations and somewhat lower haze. It is difficult to get

Table 7

Ultraviolet Scattering Haze Measured on 106 Vendor Wafers

1	100	57	141
2	112	59	117
3	93	60	132
4	119	61	138
5	131	62	171
6	124	63	193
7	124	64	148
8	140	65	138
9	137	66	154
10	77	67	146
11	111	68	109
12	128	69	135
13	138	70	113
14	75	71	133
15	116	72	133
16	113	73	139
17	118	74	131
18	111	75	133
19	127	76	144
20	110	77	140
21	150	78	141
22	72	79	147
23	117	80	133
24	142	81	137
25	85	82	135
26	130	83	111
27	145	84	131
28	87	85	136
29	126	86	130
30	147	87	130
31	110	88	130
32	139	89	130
33	137	90	110
34	153	91	110
35	153	92	115
36	137	93	120
37	138	94	130
38	148	95	112
39	138	96	130
40	134	97	130
41	131	98	131
42	143	99	131
43	143	100	131
44	143	101	131
45	143	102	131
46	143	103	131
47	143	104	131
48	143	105	131
49	143	106	131
50	143	107	131
51	143	108	131
52	143	109	131
53	143	110	131
54	143	111	131
55	143	112	131
56	143	113	131
57	143	114	131
58	143	115	131
59	143	116	131
60	143	117	131
61	143	118	131
62	143	119	131
63	143	120	131
64	143	121	131
65	143	122	131
66	143	123	131
67	143	124	131
68	143	125	131
69	143	126	131
70	143	127	131
71	143	128	131
72	143	129	131
73	143	130	131
74	143	131	131
75	143	132	131
76	143	133	131
77	143	134	131
78	143	135	131
79	143	136	131
80	143	137	131
81	143	138	131
82	143	139	131
83	143	140	131
84	143	141	131
85	143	142	131
86	143	143	131
87	143	144	131
88	143	145	131
89	143	146	131
90	143	147	131
91	143	148	131
92	143	149	131
93	143	150	131
94	143	151	131
95	143	152	131
96	143	153	131
97	143	154	131
98	143	155	131
99	143	156	131
100	143	157	131

WAFER
NUMBERHAZE
NUMBERWAFER
NUMBERHAZE
NUMBER

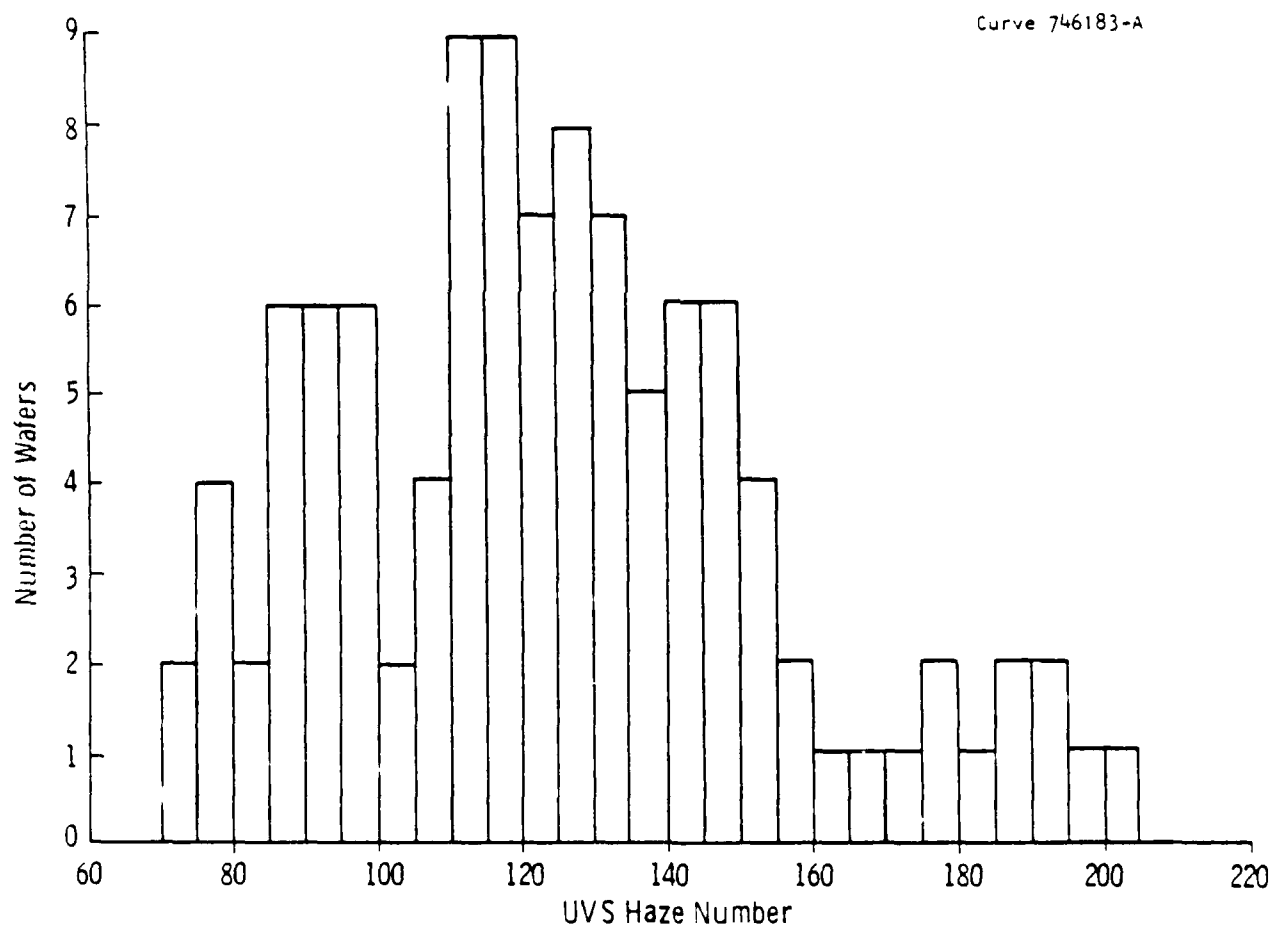


Figure 32. Histogram of the haze numbers versus haze readings for the vendor wafers.

Table 8
Summary of UVS Haze Statistics

Type of Wafer	Number	Average Haze	Max.	Min.	rms
1. Union Carbide (2-inch)	106	124.4	202	72	29.1
2. (W) Low-Temperature Epi T = 880°C	5	2666	3954	2107	660.0
3. (W) Low-Temperature Epi T = 900°C	5	1752	1890	1648	93.0
4. (W) Low-Temperature Epi T = 900°C	8	2095	2200	1820	137.0
5. (W) Epi T = 970°C	4	694	789	635	63.3
6. (W) Epi T = 970°C Kyocera Substrate	8	460	633	387	71.5
7. (W) Epi T = 1000°C	12	515	752	355	138.0
8. (W) Epi T = 1000°C	6	382	494	290	69.3
9. Union Carbide (4-inch)	8	103	170	70	33.4
10. Kyocera (4-inch)	12	37	55	20	9.6
11. Silicon Wafers	5	4.8	5	4	0.4

good epilayers at low temperature because the silicon atom surface mobility is low and the solid-phase recrystallization rate is low. Both factors interfere with the coalescence of crystallization nuclei into a single-crystal epilayer of lowest total free energy. The resulting film tends to be polycrystalline with a preferred $\langle 100 \rangle$ texture. Because the layer growth is affected by kinetic factors, the quality of the film is very sensitive to the cleanliness of the surface and the exact procedures of the growth process. Thus, at 800°C there is a very wide range and the two runs at 900°C gave slightly different average values

of the haze. The detailed surface texture, as observed by the dependence of scattering on rotation angle (see Section 3.2.5), is also significantly different from the high-temperature epilayers and vendor wafers.

The high-temperature epi runs reported as items 5-8 in Table 8 also exhibit higher haze than the vendor wafers. The reason for this difference between wafers produced under nominally near-optimal growth conditions has not been definitely established. The most probable cause is a difference in the characteristics of growth in different epitaxial reactor systems. Such a difference in characteristics has been reported based on UVR reflectance haze measurements.⁽²⁵⁾ The calibration curve relating UVR haze and microtwin density determined by X-ray pole figure analysis was shown to be quite different for SOS wafers grown in different reactors. The vendor wafers of item 1 in Table 8 were grown in an AMV 1200 pancake-type reactor, while the Westinghouse wafers were grown in an rf-heated horizontal reactor.

The prior report indicated that the SOS wafers from a horizontal reactor tended to have a higher UVR haze than wafers from a pancake or barrel reactor, at the same level of microtwin density.⁽²⁵⁾ It is also true that the vendor's system is a production facility devoted to SOS wafers, with every step of the process optimized on the basis of long experience. However, the quality of the Westinghouse wafers is comparable to the vendor wafers as measured by Raman, RBS, and as evidenced in device performance and wafer yield.

Another factor which may be significant is a difference in substrates used for the various runs. The wafers of items 5 and 7 in Table 8 were grown on sapphire substrates purchased from Union Carbide, while items 6 and 8 were grown on substrates from Kyocera. The Union Carbide substrates are sapphire crystal discs grown by the Czochralski method. Kyocera substrates are grown by the Edge Fed Growth (EFG) method. The nominal surface orientation and surface finish are otherwise the same for both substrates. In runs at the same temperature, the

Kyocera substrates give a lower average haze. However, the differences are relatively small compared to the rms variation within the runs. The numbers given in Table 8 were tested for statistical significance by using the t-test with a 0.01 level of significance. There is no statistically significant difference between items 6, 7, and 8, while item 5 does have a significantly higher haze. Within the scope of these results, then, it is not possible to conclude that the substrate has any effect on the haze number of the silicon epilayer.

Additional data are reported here on items 9 and 10 in Table 8 on wafer lots examined after the end of the investigation phase of this program. These SOS wafers were purchased as evaluation samples for Westinghouse Advanced Technology Laboratories. The Union Carbide 4-inch wafers, item 9, gave haze numbers comparable to the 2-inch wafers characterized in this program. The t-test with 0.01 level of significance shows no significant difference between items 1 and 9. However, the scattering versus rotation angle is somewhat different as reported in Section 3.2.5. The Kyocera 4-inch wafers gave much lower haze numbers than any SOS wafer previously studied. Possible reasons for this are differences in the epitaxial reactors and in the nature of the substrates.

Also shown in Table 8 are results from measurements of polished silicon wafers (item 11). The haze of such wafers, when measured with greater precision than shown in the table, is not very repeatable. The scattering versus rotation angle scans show features unrelated to crystal orientation. These results indicate that although the silicon surface is much smoother and less hazy than any SOS wafer, the scattering is dominated by accidental features such as dust or scratches.

3.2.4.4 Comparison of EVS and EVR Haze Measurements

Another optical method for characterizing SOS wafers has been reported recently.⁽²⁶⁾ This method is based on the Ultraviolet

Reflectance (UVR) of the silicon epilayer. It has been shown that the specular reflectivity at 280 nm wavelength depends on the perfection of the silicon crystal.⁽²⁷⁾ A damaged surface or an amorphous silicon layer reflects less light at this wavelength than a damage-free polished silicon wafer. The reflectivity decrement at 400 nm is subtracted from the decrement at 280 nm to compensate for surface roughness. The final haze number is intended to indicate crystal quality as opposed to surface topographical effects.

At the time the SOS wafers were ordered for this program, the vendor had installed an instrument to measure UVR haze. The haze numbers were to be used as a process monitor to detect increases in haze which would signify a problem arising in the process. The vendor agreed to supply us with the UVR haze readings for all of the wafers we purchased for comparison with our characterization results. These readings are shown in Table 9.

The UVR haze numbers are compared with the UVS haze numbers in Figure 33. There is a weak correlation in that wafers with higher vendor UVR haze numbers tend to show higher UVS haze also. The agreement is far from satisfactory at every level, and especially at zero-indicated UVR haze, where the UVS measurements show a very substantial range from the lowest to the nearly highest values observed. The comparison in Figure 33 clearly shows some methodological differences between UVS and UVR haze techniques. The UVS scattering method always gives a definite number for the haze. This number is reasonably repeatable upon removing and replacing the wafer, and is not overly sensitive to surface films or dust. The UVR haze data have a much coarser resolution, with many wafers registering zero haze or negative haze numbers which are assigned to zero to avoid apparently unphysical values. The poor resolution of UVR haze can be attributed to lack of precision in the measurement. In the UVR technique, the reflected signal from the SOS wafer is measured, and the reflected signal from a silicon standard is measured. It is the difference between these signals, normalized to account for system gain, that

1. The first step in the process of the investigation is the identification of the problem. This is done by the investigator who is responsible for the investigation. The investigator must identify the problem and the scope of the investigation. This is done by the investigator who is responsible for the investigation.

2. The second step in the process of the investigation is the collection of data. This is done by the investigator who is responsible for the investigation. The investigator must collect data that is relevant to the problem and the scope of the investigation. This is done by the investigator who is responsible for the investigation.

3. The third step in the process of the investigation is the analysis of the data. This is done by the investigator who is responsible for the investigation. The investigator must analyze the data to determine the cause of the problem and the scope of the investigation. This is done by the investigator who is responsible for the investigation.

4. The fourth step in the process of the investigation is the development of a solution. This is done by the investigator who is responsible for the investigation. The investigator must develop a solution that addresses the problem and the scope of the investigation. This is done by the investigator who is responsible for the investigation.

5. The fifth step in the process of the investigation is the implementation of the solution. This is done by the investigator who is responsible for the investigation. The investigator must implement the solution and monitor the results of the investigation. This is done by the investigator who is responsible for the investigation.

6. The sixth step in the process of the investigation is the evaluation of the results. This is done by the investigator who is responsible for the investigation. The investigator must evaluate the results of the investigation to determine the effectiveness of the solution. This is done by the investigator who is responsible for the investigation.

7. The seventh step in the process of the investigation is the documentation of the results. This is done by the investigator who is responsible for the investigation. The investigator must document the results of the investigation and the solution. This is done by the investigator who is responsible for the investigation.

8. The eighth step in the process of the investigation is the dissemination of the results. This is done by the investigator who is responsible for the investigation. The investigator must disseminate the results of the investigation to the appropriate parties. This is done by the investigator who is responsible for the investigation.

9. The ninth step in the process of the investigation is the follow-up. This is done by the investigator who is responsible for the investigation. The investigator must follow-up on the results of the investigation and the solution. This is done by the investigator who is responsible for the investigation.

10. The tenth step in the process of the investigation is the conclusion. This is done by the investigator who is responsible for the investigation. The investigator must conclude the investigation and the solution. This is done by the investigator who is responsible for the investigation.

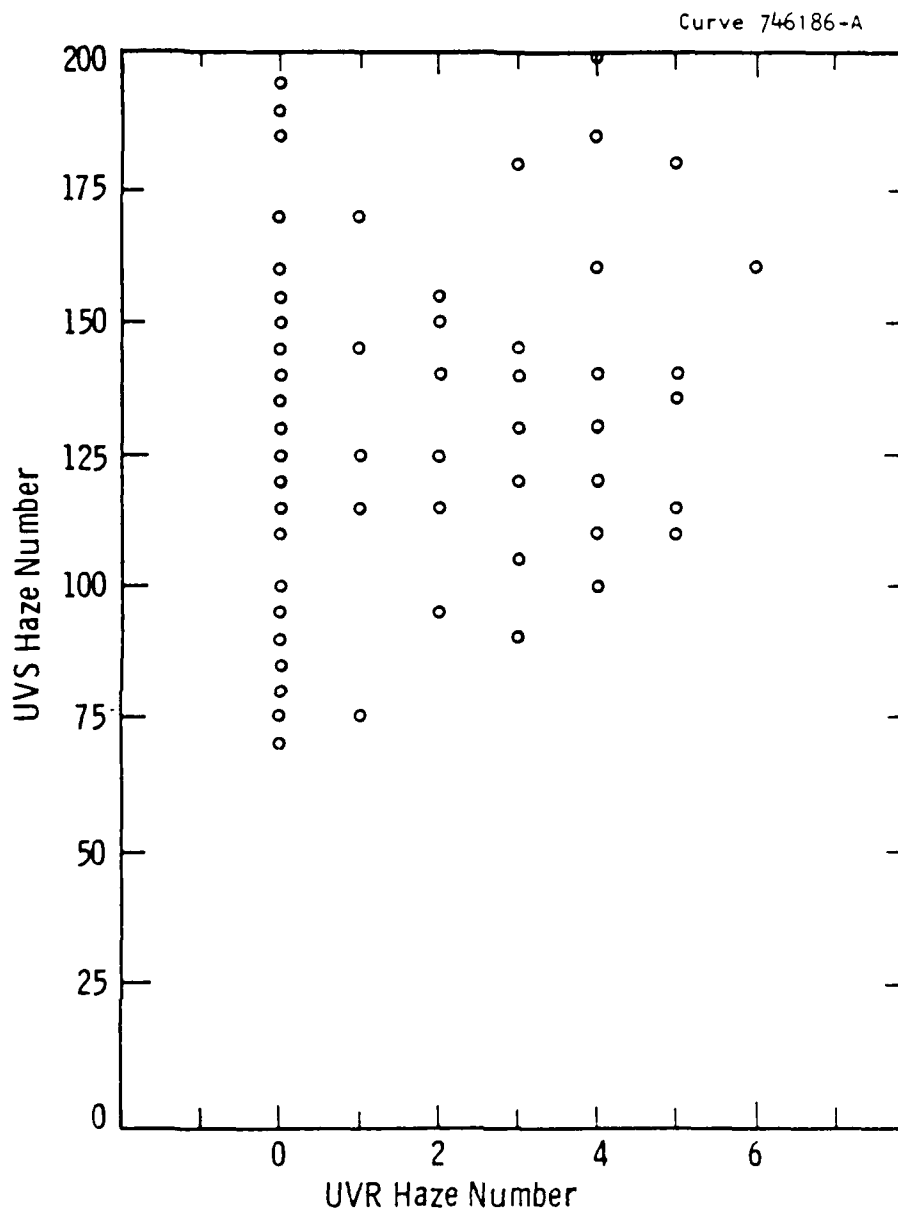


Figure 33. Westinghouse haze readings from UV scattering plotted versus vendor haze readings from UV reflectivity for 105 vendor wafers.

constitutes the reflectivity characteristic at one wavelength. This difference is a relatively small number compared to the signal being measured. To get the haze number, the difference is taken between readings at 280 and 400 nm. Thus, the final haze number is the difference of two differences or the difference of two numbers, each of which is small compared to the quantity measured. With such a double subtraction, the requirements on the accuracy of the initial measurements of the reflected light signals are very great. In comparison, for the UVS scattering technique, the quantity being measured is very small. The scattered light signal is many orders of magnitude smaller than the reflected light signal, but it is measured directly by a very sensitive detection system. The precision of the UVS haze number is then directly the precision of measuring a small signal, with no necessity of finding a difference of small numbers.

3.1.5 UVS Rotation Angle Scans

Rotations of the SOS wafer under test were initially done to determine whether the measured haze number was unduly sensitive to wafer position or orientation. A few selected wafers showed some dependence of scattering on wafer rotation angle, but the magnitude of the variation was not large enough to interfere with the haze measurement. Later, during the course of the investigation, the haze apparatus was reconfigured to measure the scattering as a function of rotation angle through a full 360° revolution. A surprising variety of results were obtained, with scattering peaks of considerable amplitude being found at different angles on different wafers. This led to a more detailed investigation of this phenomenon as a means of obtaining more information on the origin and interpretation of haze as related to silicon epilayer surface texture. Unfortunately, the investigation of rotation angle scans occurred after the last wafers were submitted for processing, so there is no data base for correlating angular dependence of scattering with device yield. However, this type of measurement led

us to insights on the nature of the silicon surface, and may prove to be a useful tool for further more detailed investigations.

The dependence of scattering on rotation angle was measured using the setup diagrammed in Figure 34. The sample is held in a vertical plane with the silicon surface perpendicular to the axis of the incident beam. This ensures that the specular reflection is directed back along the axis of the incident beam. The detector is located at a fixed angle of 30° with respect to the incident beam axis. This scattering angle is greater than that used for the haze measurements. The sample is rotated about the beam axis by the indexing rotary table which holds the vacuum fixture. The rotation angle θ is positive for clockwise rotations viewed from the silicon surface of the SOS wafer. The zero reference for θ is established by resting the wafer on the flat before applying vacuum.

Rotation angle scans are shown for two SOS vendor wafers in Figure 35. The intensity of the scattered light is seen to depend strongly on the rotation angle. Each wafer shows two peaks in the scattered intensity at angles that are 180° apart. The results shown for W78 are typical of a large number of vendor wafers which we denote as Type I. The first peak of a Type I curve appears after a rotation of $35 \pm 5^\circ$ and the second peak is 180° away from the first. Wafer W82 is typical of Type II wafers, with a first peak at $125 \pm 5^\circ$. These scattering curves are surprising in two respects. First, the two-fold or mirror symmetry implied by the peaks spaced 180° apart seems to contradict the nominal four-fold symmetry expected from a 100 silicon surface. The epilayer orientation has been well established as 100 in many investigations and confirmed by reflection electron diffraction for selected wafers in this study. Small deviations from exact orientation would not be expected to produce the very pronounced two-fold scattering pattern observed. The exact cause of this change in surface symmetry is not yet understood. Secondly, the existence of two types of wafers in a nominally identical set of samples was surprising. This effect has been traced to the orientation of the sapphire substrate.

AD-A150 004 FACTORS AFFECTING SOS (SILICON-ON-SAPPHIRE) YIELD AND
RELIABILITY. (U) WESTINGHOUSE RESEARCH AND DEVELOPMENT
CENTER PITTSBURGH PA P G McMULLIN JUL 84
UNCLASSIFIED 83-6F4-FACTR-R1 RAD-TR-84-115 F/G 9/1

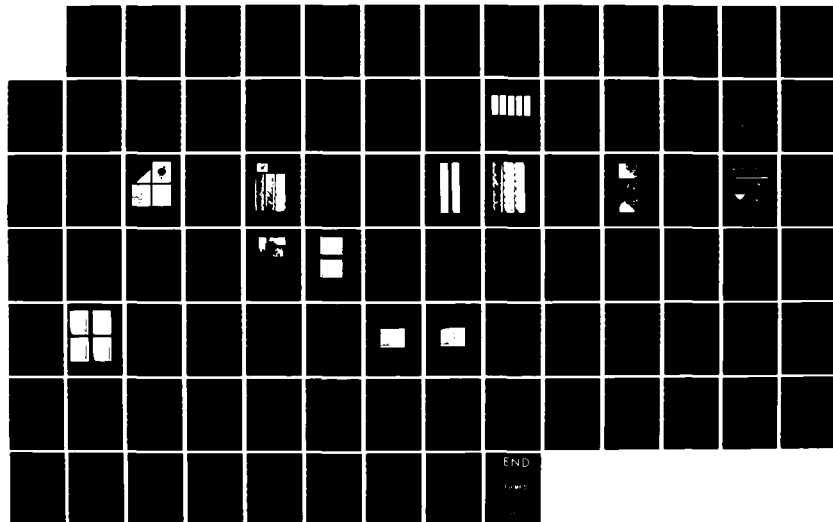
FACTORS AFFECTING SOS (SILICON-ON-SAPPHIRE) YIELD AND
RELIABILITY. (U) WESTINGHOUSE RESEARCH AND DEVELOPMENT
CENTER PITTSBURGH PA P G MCMULLIN JUL 84
83-6F4-FACTR-R1 RADC-TR-84-115 F/G 9/1

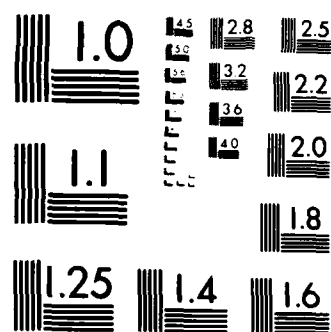
2/2

UNCLASSIFIED

F/G 9/1

NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

Dwg. 9357A50

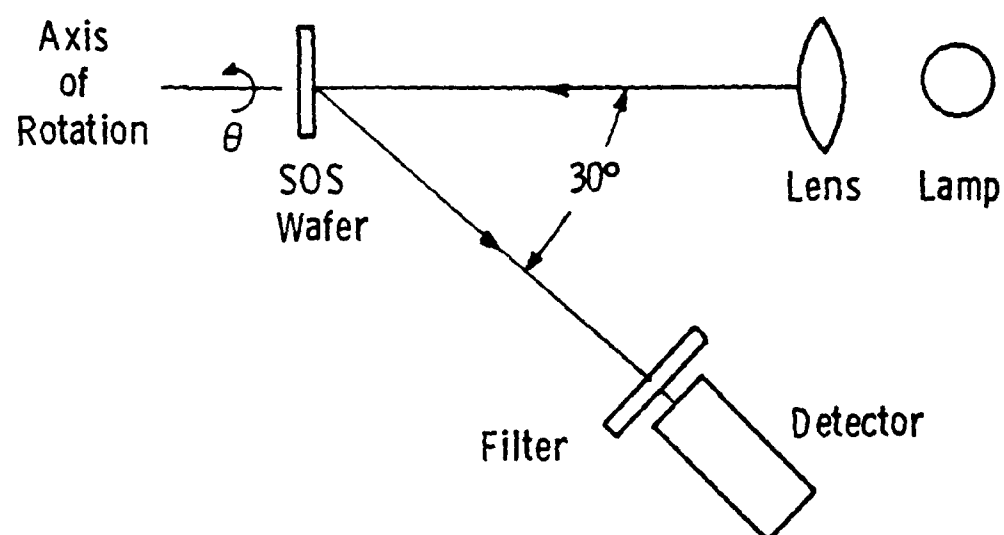


Figure 34. Setup for UV scattering haze angular dependence.

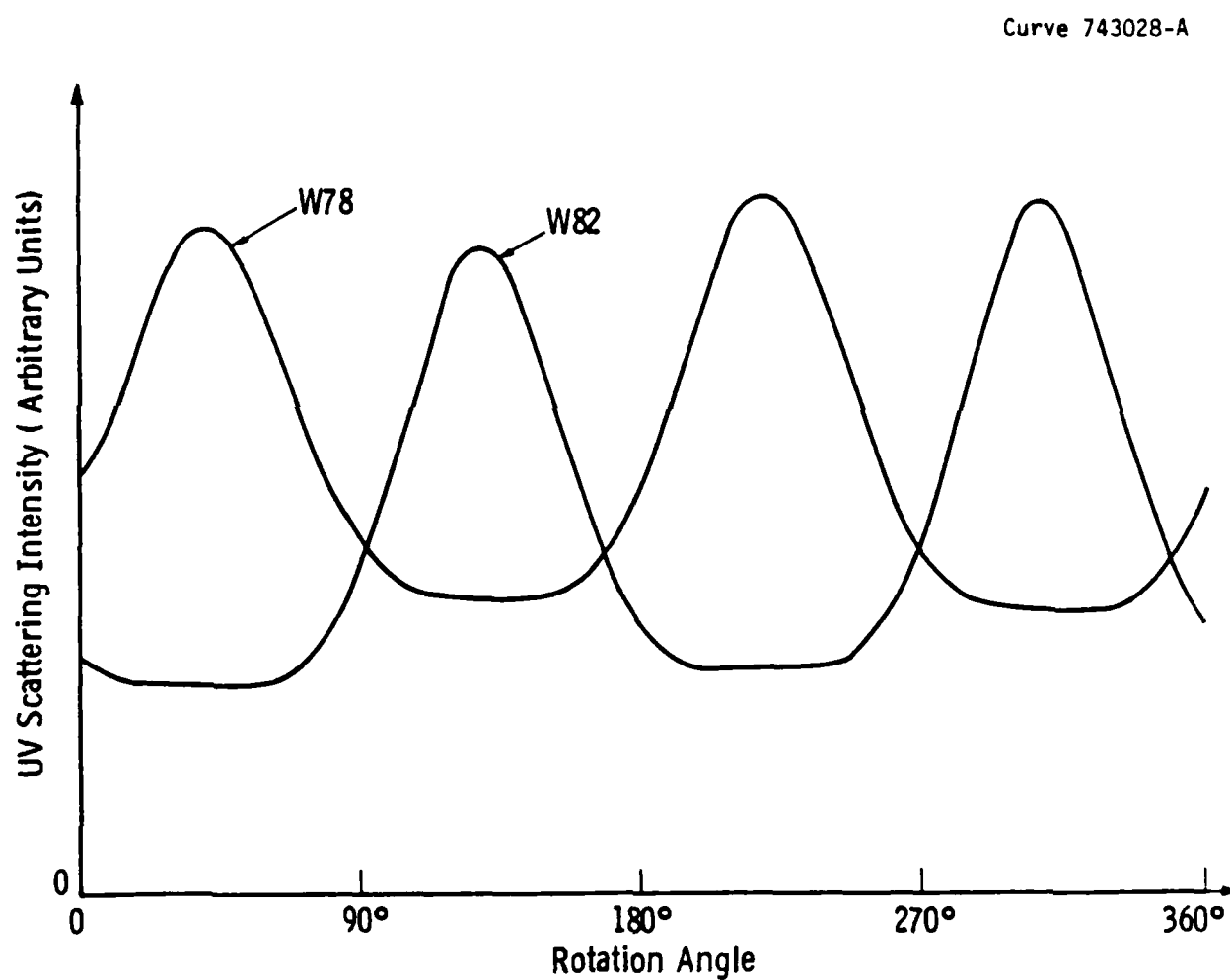


Figure 35. UV scattering versus rotation angle for two vendor SOS wafers.

Wafers of Type I and Type II were oriented by X-ray diffraction as described in Section 2.4. It was found that the two types differ in the orientation of the c-axis projection with respect to the wafer plot. For Type I wafers, the c-axis projection lies 45° counterclockwise from a line connecting the center of the wafer and the center of the plot. Type II wafers have the c-axis projection located 45° clockwise from the flat. This difference in orientation probably arose in preparation of the sapphire substrates, with the Type II wafers being flipped over with respect to the Type I wafers before polishing one surface for epi deposition. The correlation of substrate orientation and wafer type can also be confirmed in the wafer bow photographs. The two-inch SOS wafers typically show an axis of symmetry in the bow interferograms, with the axis located $\pm 45^\circ$ from the wafer flat. In every case in which a symmetry axis could be observed, the axis was 45° counterclockwise from the flat for Type I wafers; and 45° clockwise for Type II wafers. SOS wafer bow arises from the differential thermal contraction of the epilayer and substrate upon cooling from the growth temperature. The elastic properties of the epilayer are symmetric in the plane of the layer because of the 100 orientation of the layer. The elastic constants of the substrates depend upon orientation since the substrate lacks symmetry. The wafer bow interferograms indicate a greater curvature along a line perpendicular to the c-axis projection. The silicon epilayer compressive stress is therefore greater along this line. It may be possible that this asymmetrical stress has caused a change in the epilayer surface, perhaps through deformation during cooling, that in turn gives rise to the unusual scattering peaks.

The orientation of the scattering peak with respect to the c-axis projection was determined by measurement. The placement of the detector in the set-up shown in Figure 34 is constrained by other apparatus so that the detector lies slightly above a horizontal plane passing through the center of the wafer. The angle of elevation was calculated to be 1° and this was confirmed by experiment. A plane mirror was mounted on a 15° wedge and placed in the position of the

wafer under test. The mirror was aligned so that the reflection of the incoming beam was in a vertical plane by adjusting the mirror until the reflection and the incoming beam itself both intersected a plumb line. The detector output showed a peak after a rotation of 80° , confirming that the detector was elevated by 10° from the horizontal. We can now interpret the location of the first peak of Type I wafers. The peak occurs at 35° of rotation. If the detector were in the horizontal plane, the peak would come in at 45° of rotation. Since the c-axis projection is 45° CCW from the plot, a 45° CW rotation will place the c-axis in a vertical plane when the scattering peak is seen in the horizontal plane. Thus, the scattering peaks are observed at 90° angles from the c-axis projection, within the $\pm 5^\circ$ precision of measurement.

The scattering was measured at several wavelengths by inserting narrow-band interference filters in front of the detector. Figures 36 and 37 show the results for W78 and W82. The broadband curve is taken with no filter in place. The wavelength response is dictated by the photomultiplier tube, which is insensitive to wavelengths longer than 350 nm. The curves at 280 and 200 nm are similar, except that the contrast or peak-to-valley ratio is greater at 200 nm. Also, there is a trace of additional structure in the form of weak peaks at 90° away from the strong peaks. For some of the vendor wafers, the subsidiary peaks are more pronounced than those observed in Figure 36.

The scattering from the Westinghouse epilayers differs from that of the vendor wafers. The high-temperature epilayers ($T = 970$ or 1000°C) typically show four peaks, as seen in Figure 38. The scattering is similar at 200 nm, 280 nm, and broad band, except that the contrast ratio is higher at 200 nm. The location of the first peak is locked to the substrate orientation, as it was for the vendor wafers. Since there are four equivalent peaks, there is no significance in the c-axis projection lying on one side of the flat as opposed to the other. The magnitude of the scattering signal is much higher for the Westinghouse wafers, as discussed in the UVS haze data section. The scattering results are very similar for epilayers grown on Union Carbide and Kyocera substrates.

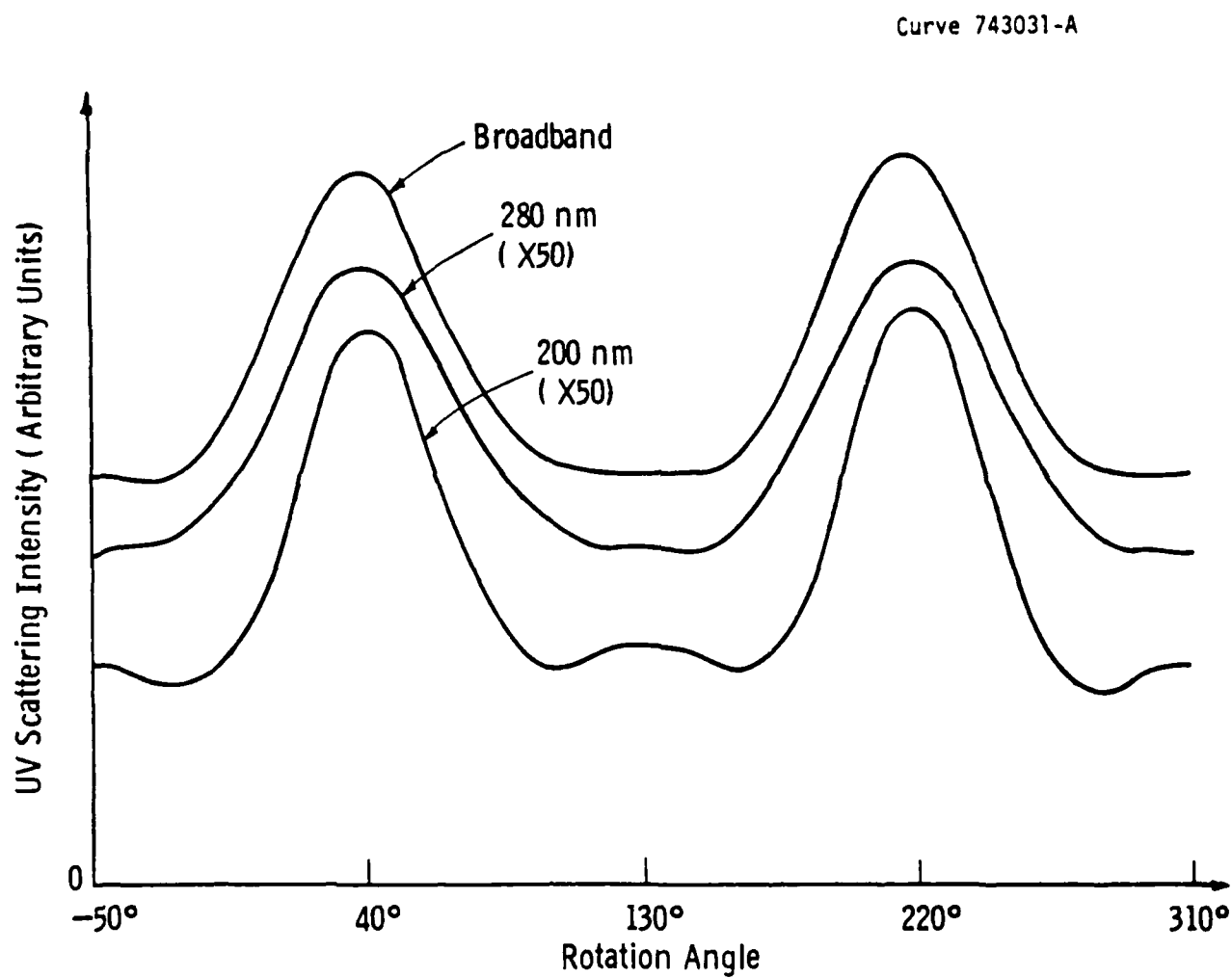


Figure 36. UV scattering versus rotation angle as a function of UV wavelength for vendor wafer W78. The scan starts at 50°C CCW from the zero reference angle, or nominally 90° before the first major peak.

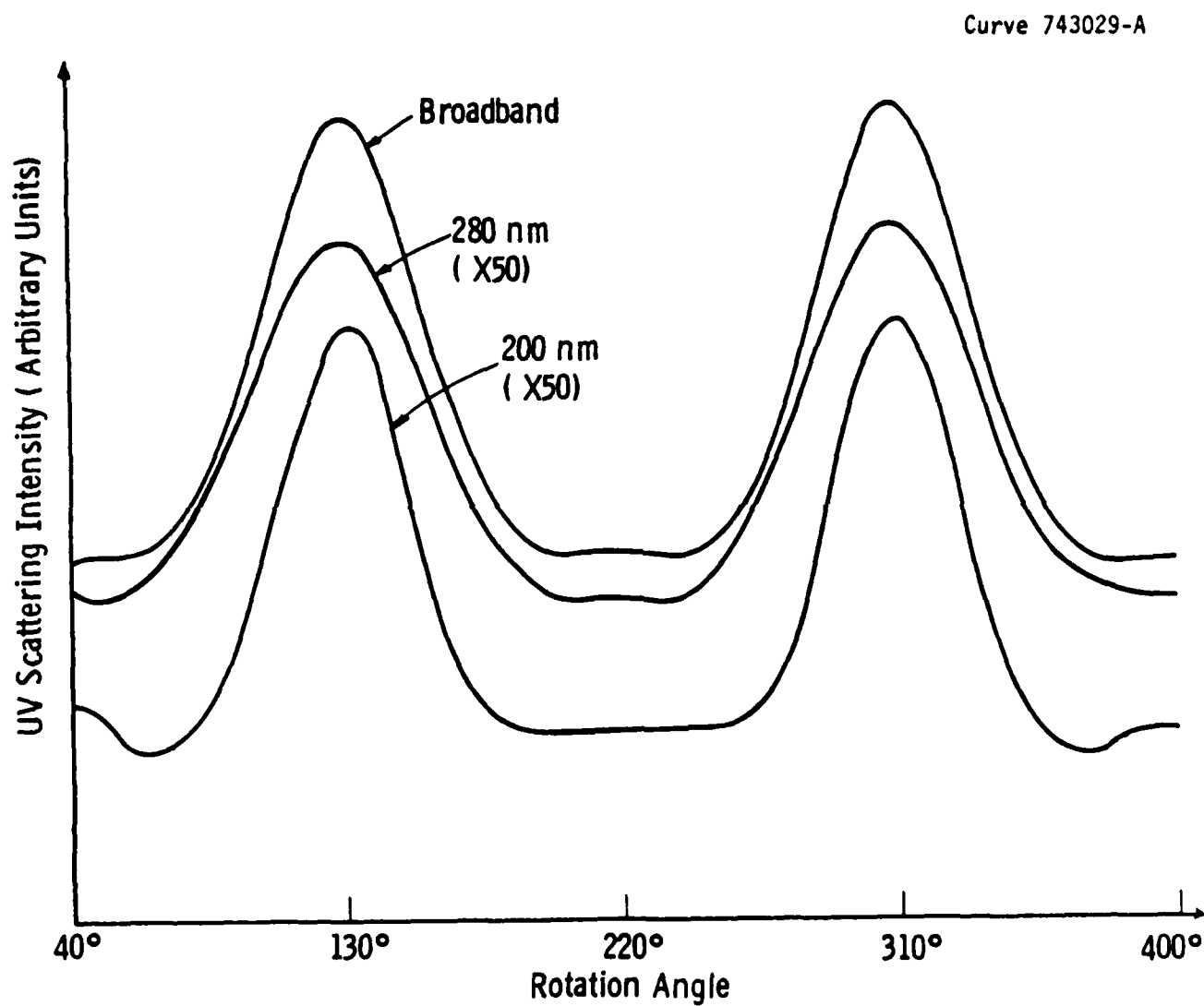


Figure 37. UV scattering versus rotation angle as a function of UV wavelength for vendor wafer W82. The scan starts at 40°, or nominally 90° before the first major peak.

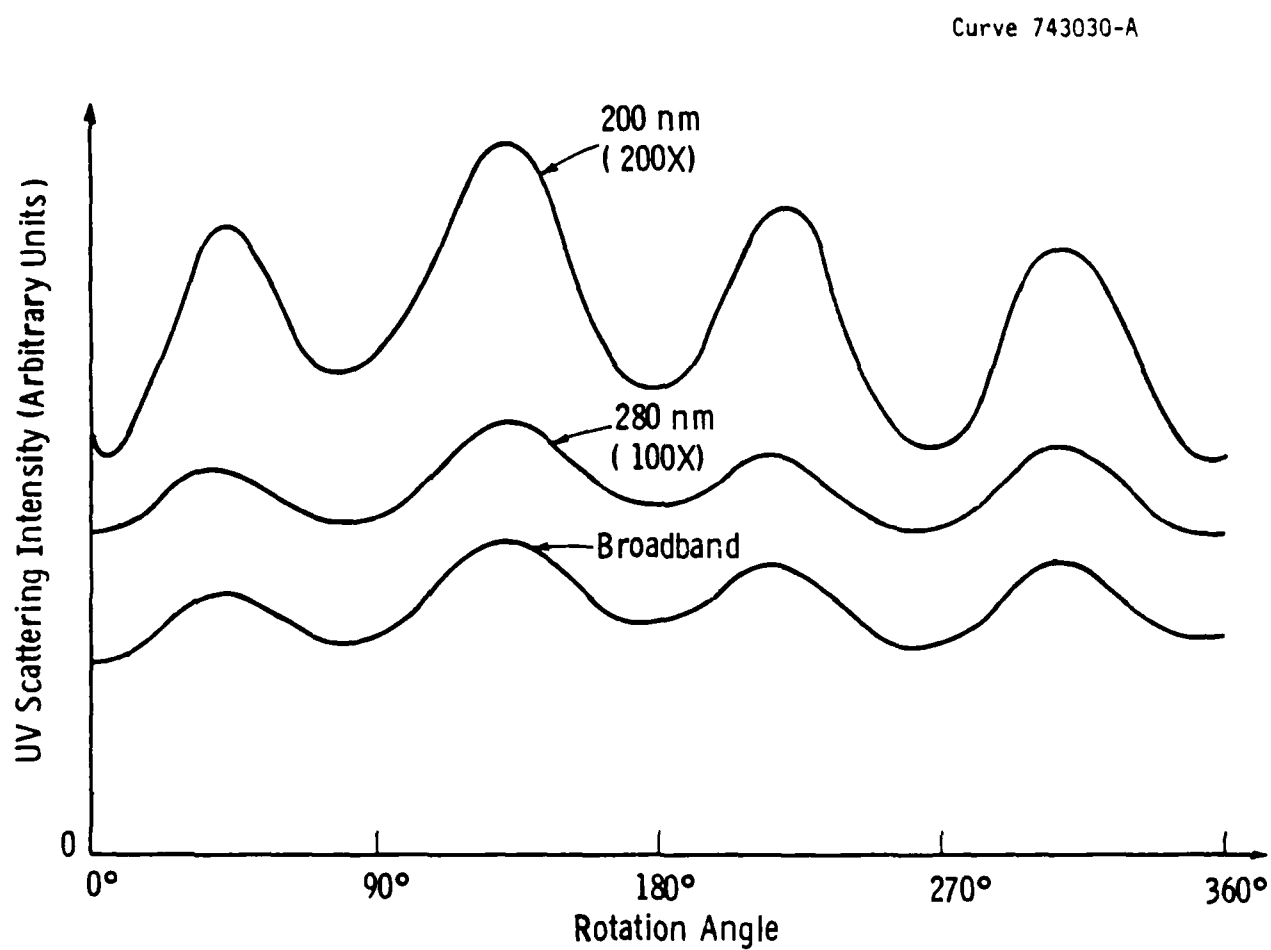


Figure 38. UV scattering versus rotational angle as a function of UV wavelength for Westinghouse epi wafer W401.

The low-temperature epilayers produce yet another type of scattering versus rotation angle. Figure 39 shows the scattering from a layer deposited at 880°C. The signal is higher in magnitude than for the vendor wafers and the high-temperature epilayer, and is relatively featureless. Although there are typically two maxima, the peaks are very broad and the maxima do not occur at characteristic angles.

The UV scattering versus rotation angle was also measured on some 4-inch SOS wafers acquired after the nominal end of the investigation of this program. These wafers were evaluation samples purchased by Westinghouse Advanced Technology Laboratory and characterized for UVS haze before processing. The results for Kyocera wafers are shown in Figure 40. Nineteen wafers were examined. Of these, five showed substantial secondary peaks between the two major peaks. One wafer, shown as No. 19 in Figure 40 exhibited four equivalent peaks. Most of the wafers, as wafer no. 9 in Figure 40, had two major peaks with an unusually high contrast ratio. All of the wafers were nominally Type II with the first major peak coming in at about 130° rotation angle. The amplitude of scattering was low: these Kyocera wafers had the lowest UVS haze of any SOS wafers examined thus far.

Eight 4-inch wafers from Union Carbide were also examined. The range of results are indicated in Figure 41. In this group, four of the wafers had four equivalent peaks, and only one wafer had two strong peaks with no apparent secondary peaks. These cases are shown as wafer No. 8 and wafer No. 1, respectively, in Figure 41. The magnitude of the scattering was in the same range as the 2-inch SOS Union Carbide wafers previously described.

This concludes the description of the rotation angular dependence of UV scattering on unmodified SOS wafers. In the next section, several experiments are described which were designed to determine the origin of UV scattering.

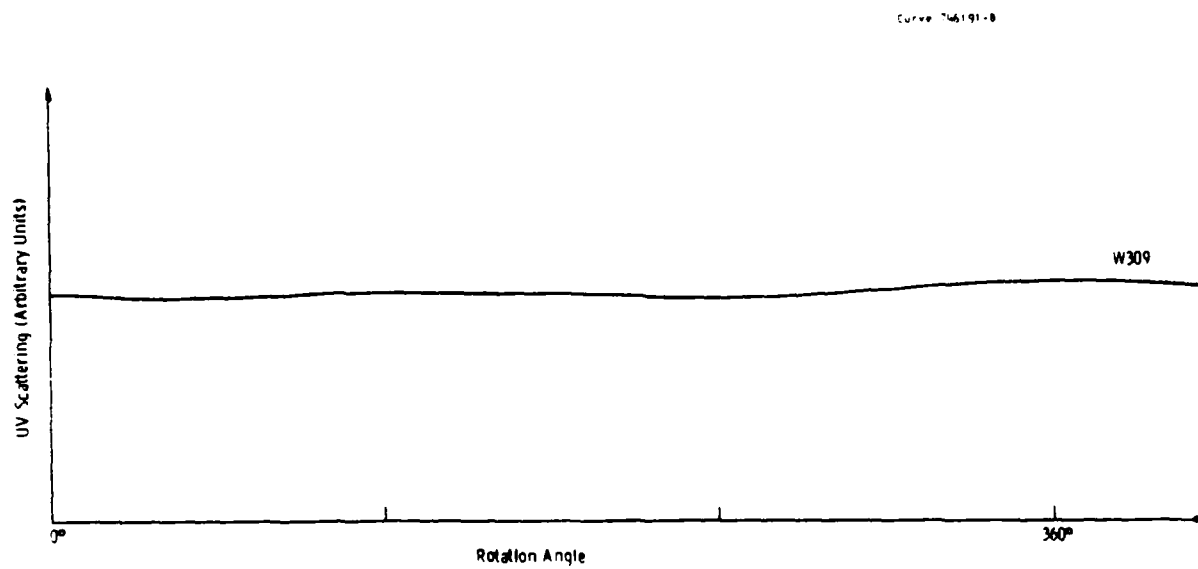


Figure 39. UV scattering versus rotation angle for low-temperature epi wafer W309.

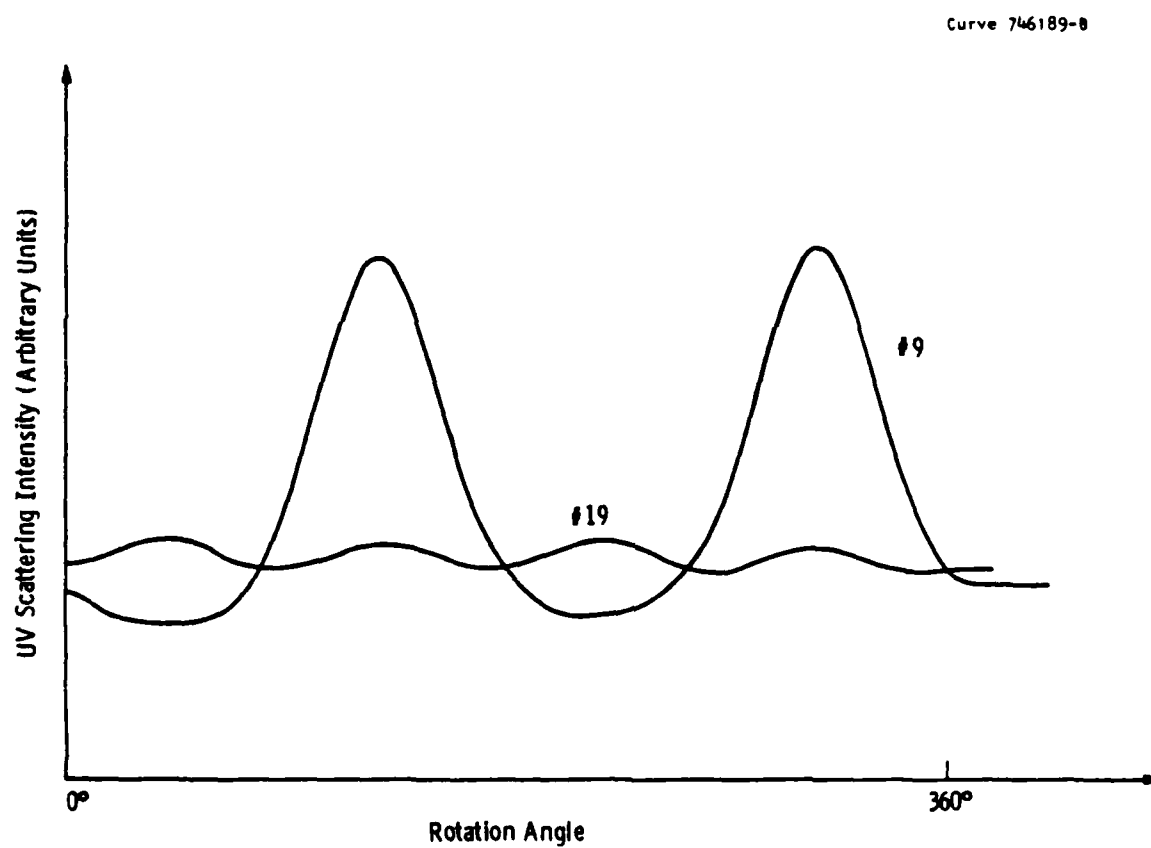


Figure 40. UV scattering versus rotational angle for two Kyocera 4-inch SOS wafers.

Curve 746192-8

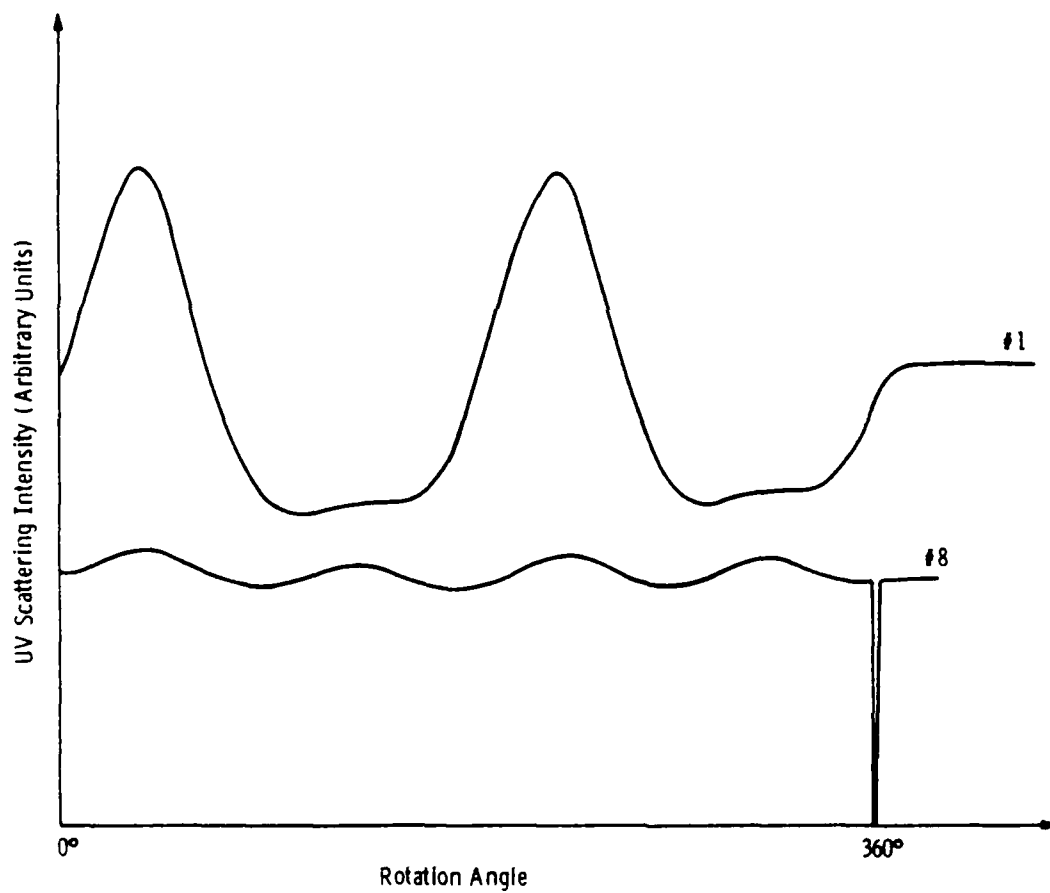


Figure 41. UV scattering versus rotation angle for Union Carbide 4-inch SOS wafers.

3.2.6 Sources of UVS Haze

The following sources of scattering were considered: scattering by nonlinear processes which involve a wavelength shift such as fluorescence; scattering from optical inhomogeneities in the bulk of the silicon, and scattering from surface asperities. Experimental results show that the scattering is due to surface features that are present on the silicon epilayer and absent on the substrate.

The intensity of scattering due to wavelength shifting processes such as fluorescence was evaluated by changing the position of the narrow-band filter in the beam path. When the 280 nm narrow-band filter is placed at the detector aperture, the full, wide-band output of the mercury arc lamp strikes the sample. Wavelengths shorter than 280 nm could stimulate fluorescence at 280 nm that would pass the filter at the detector. Wavelength components in the incoming beam with longer wavelengths could only contribute very weak upshifted scattering by anti-stokes Raman scattering, for example. The total signal due to nonlinear scattering would be the convolution of the optical intensity versus wavelength with the scattering response at 280 nm to the given input wavelength. Because the input beam is unfiltered and full intensity at the sample, a relatively large signal would be expected.

When the 280 nm filter is placed at the arc lamp, only a much less intense, narrow-band beam strikes the sample. The signal from the detector will be proportional to the nonlinear response to the 280 nm incoming beam, integrated over all wavelengths within the sensitivity range of the detector. A relatively small signal would be expected. Detailed calculations of expected intensities are not required, since the experiment is meant only to discover whether the scattering in the two cases is measurably different. The measurements show that the scattering signal differs at most by 3% when the filter position is changed. This shows that the contribution to scattering by nonlinear processes such as fluorescence is negligible.

Scattering can also be caused by imperfections in the material which give rise to local variations in the optical properties. Possible sources of such local changes would be crystal defects or doping fluctuations. Variations in the intensity and phase of the reflected light could cause very substantial scattering through diffraction effects. This type of scattering can only occur near the surface of the silicon epilayer, because the UV wavelength we are using does not penetrate very far. Figure 42 shows the absorption length in crystalline silicon from recent data.⁽²⁸⁾ Only features in the top 10 to 20 nm of the silicon epilayer will give scattering that will be detected by the solar-blind photomultiplier tube. An experiment was performed to determine whether optical inhomogeneities are a major cause of UVS haze. A layer of aluminum 50 nm thick was evaporated onto the surface of an SOS wafer. The aluminum layer was thick enough to prevent any UV light from reaching the surface of the silicon epilayer. The results are shown in Figure 43. The rotation angle scan shows the same pattern of scattering. The amplitude of scattering is similar, being slightly higher for the aluminized wafer due to the higher reflectivity of the aluminum. This experiment proved that the major features of UVS haze must be due to surface asperities.

Asperities at the silicon surface could originate during the growth of the epilayer, or they could be simply substrate surface features replicated at the silicon surface. To check this possibility, the rotation angle scattering was measured on six SOS wafers. The silicon surfaces were metallized by evaporating a thin layer, and the rotation angle scans were repeated. The silicon epilayers were then stripped off by hydrofluoric-nitric-acetic acid wet etch. The sapphire substrates were then metallized by evaporating 100 nm of silver or palladium onto the polished surface. Aluminum was also tried as a surface metallization but did not adhere well. The rotation angle scattering of the metallized substrates was measured. The results are shown in Figure 44. None of the six substrates showed the characteristic two or four-peak scattering patterns observed on the SOS wafers.

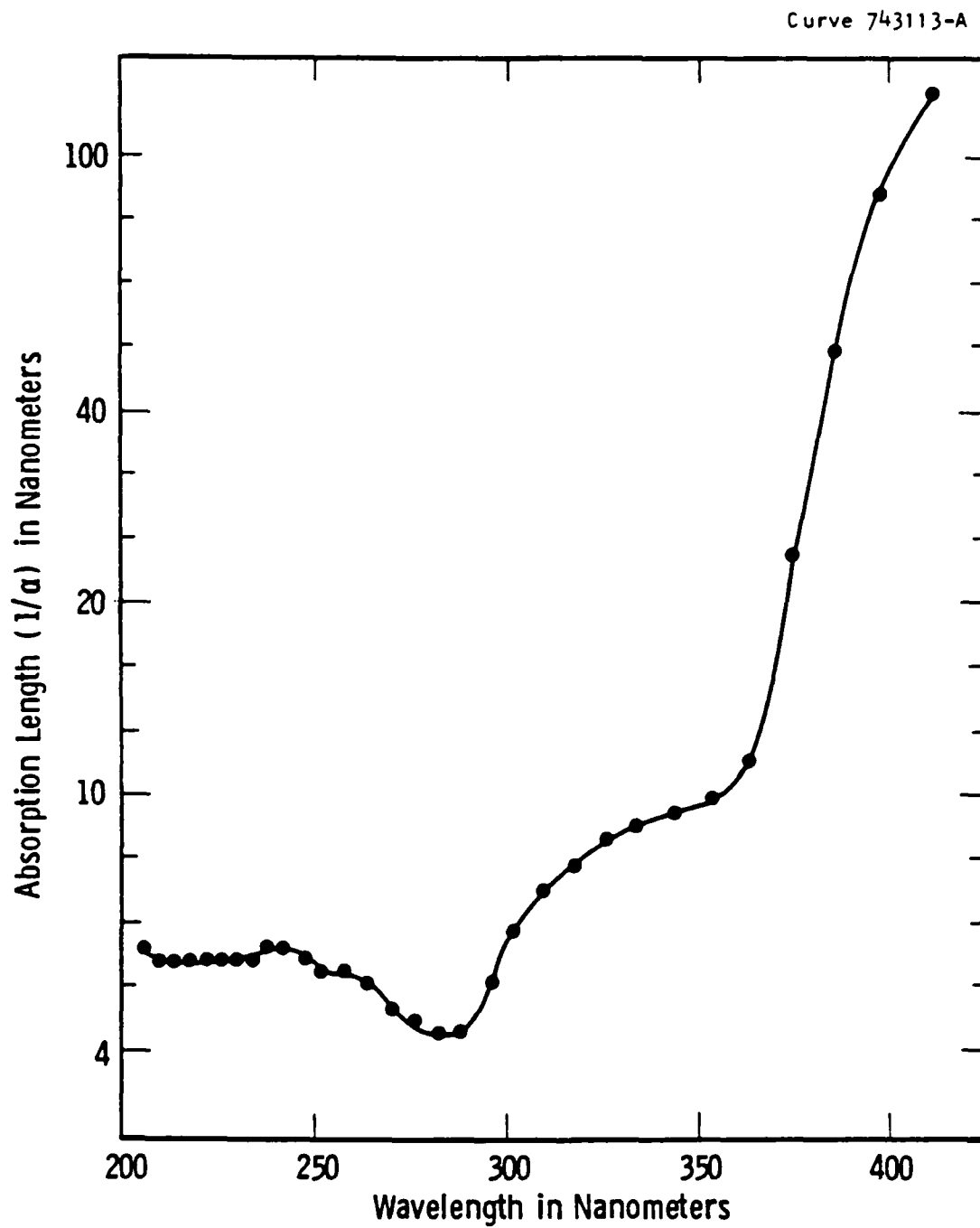


Figure 42. Silicon optical data from Aspnes and Studna.

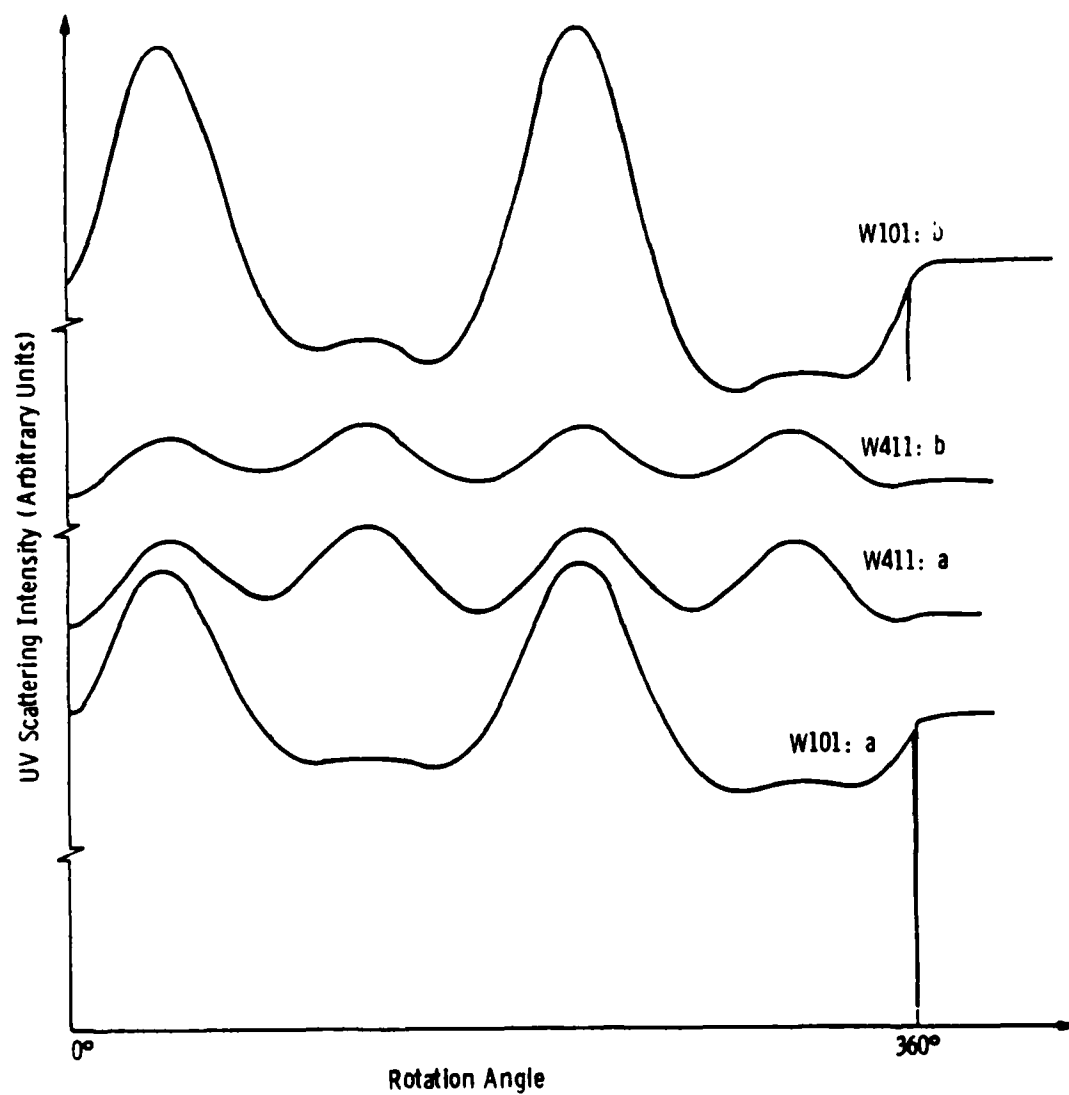


Figure 43. UV scattering versus rotation angle: a) SOS wafers with bare silicon surface, b) same wafers after evaporation of 50 nm aluminum onto surface.

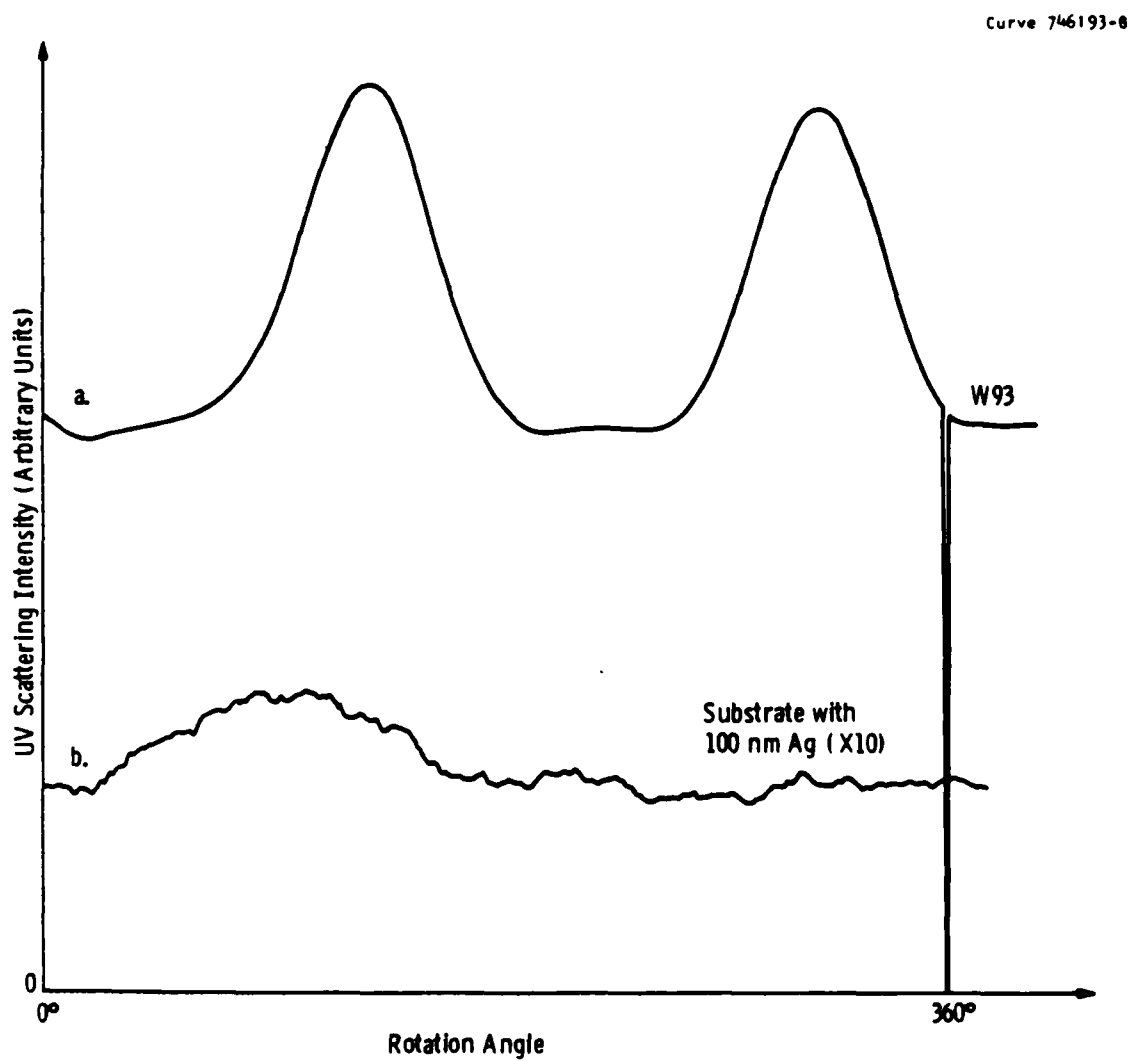


Figure 44. UV scattering versus rotation angle: a) W93 with 50 nm of aluminum on surface, b) substrate of W93 with 100 nm of silver on surface.

The lower amplitude of the haze from the metallized substrate is partly due to the lower reflectivity of silver in the UV, but also indicates that the substrate is smoother than the epilayer.

When it was determined that surface features are the cause of the rotation angle scattering peaks, we began an investigation of the nature of the surface texture. This investigation was not anticipated in the program plan, and the program resources did not allow this to be carried to completion. The strong scattering peaks at 90° orientation from the c-axis projection suggest an array of linear features on the surface. It was confirmed that a linear array will cause such scattering by fabricating a stripe pattern on an SOS wafer.

The stripes were about 1 mm long and varied in width from 3 to 5 μm . The stripes were defined in photoresist and the exposed silicon was wet etched to the substrate. The resulting angular scattering figure is shown in Figure 45. Two major peaks are seen at $150-170^\circ$ and $320-350^\circ$ of rotation. Taking account of the 10° elevation of the detector above the horizontal plane, this agrees well with scattering maxima at 90° from the stripes, which were oriented vertical with respect to the wafer flat. The reason for the fine structure within the scattering peaks is not known.

Experiments were undertaken to observe the surface texture by means other than haze measurements. Cross-section TEM measurements are described in Section 4.1. Talystep mechanical measurements of surface roughness were taken on several wafers. Optical micrographs were taken at high magnification using the Nomarski phase differential interference contrast method. The results are described below.

Talystep measurements are made by tracing surface contours with a stylus that is extremely sensitive to vertical displacements. As the sample is traversed horizontally on the sample stage, the Talystep machine produces a tracing that represents the surface of the sample. Such traces were taken on several wafers that exhibited pronounced peaks in the UV rotation angle scattering. Scans were taken both along the

Curve 746190-8

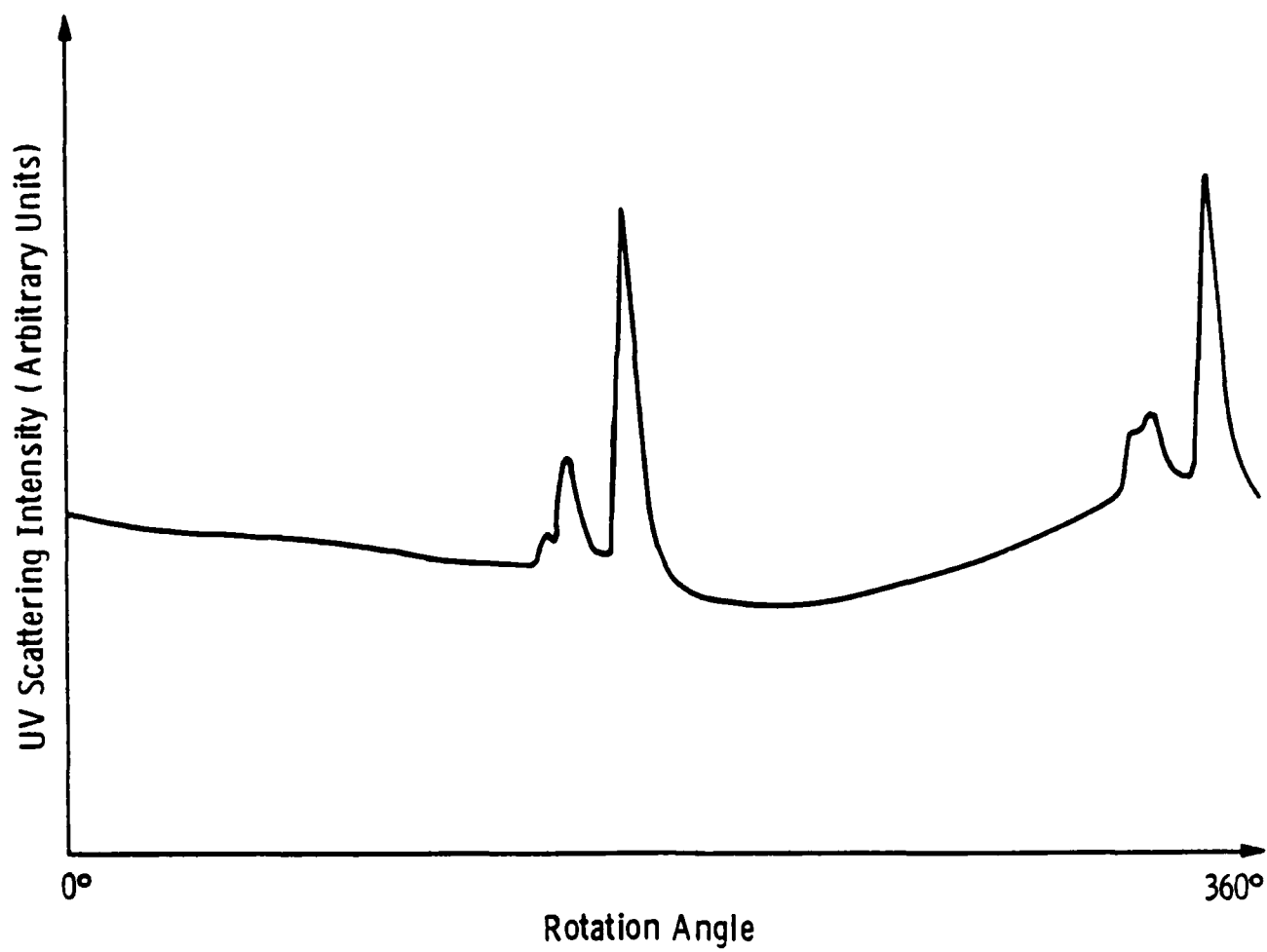


Figure 45. UV scattering versus rotation angle for a sample with a stripe pattern fabricated on the surface.

c-axis direction, 45° away from the flat, and perpendicular to the c-axis. A difference in the texture measured along these axes would be consistent with the existence of linear features giving rise to the scattering. Typical traces are shown in Figure 46. The noise level is 4 nm, peak to peak. There is a slight difference in the apparent surface roughness between the two traces. The scan perpendicular to the c-axis is smoother, with about 2 nm average and 3 nm peak deviations. The major peak in this trace was due to a door closing in a nearby room. The scan parallel to the c-axis is rougher, with about 3 nm average and 4 nm peak deviations. The lateral resolution of this technique is limited by the 12.5 μm radius of the stylus. Features smaller than about 10 μm in lateral extent will not be clearly resolved in Talystep scans. Although these results are consistent with a directional surface texture, the data are so close to the noise level that it is not possible to state a firm conclusion.

The Nomarski technique of optical microscopy is very effective for examination of polished surfaces. By adjustment of the objective lens attachment the plane surface can be made dark, while deviations from planarity show up as bright features. Several SOS wafers were examined by Nomarski optical microscopy. A Zeiss Ultraphot microscope was used, with an 80X objective lens. Illumination by a tungsten filament lamp was not bright enough to show any surface details with the objective set for surface extinction. A Cesium iodide arc lamp was used to get higher brightness. The photos in Figure 47 illustrate the results. A silicon wafer gives very little contrast, even with the bright light source. The vendor SOS wafers show a definite granularity. There is no clearly discernible pattern on the surface that is consistent with linear features aligned along the c-axis. However, if the sample is rotated, the brightness of the image changes. (The brightness change is detectable by human eye.) This was confirmed by using the microscope photometer to measure the exposure time and function of rotation angle. Exposures ranged from 8 to 12 seconds, showing a single maximum at 180° rotation from a single minimum.

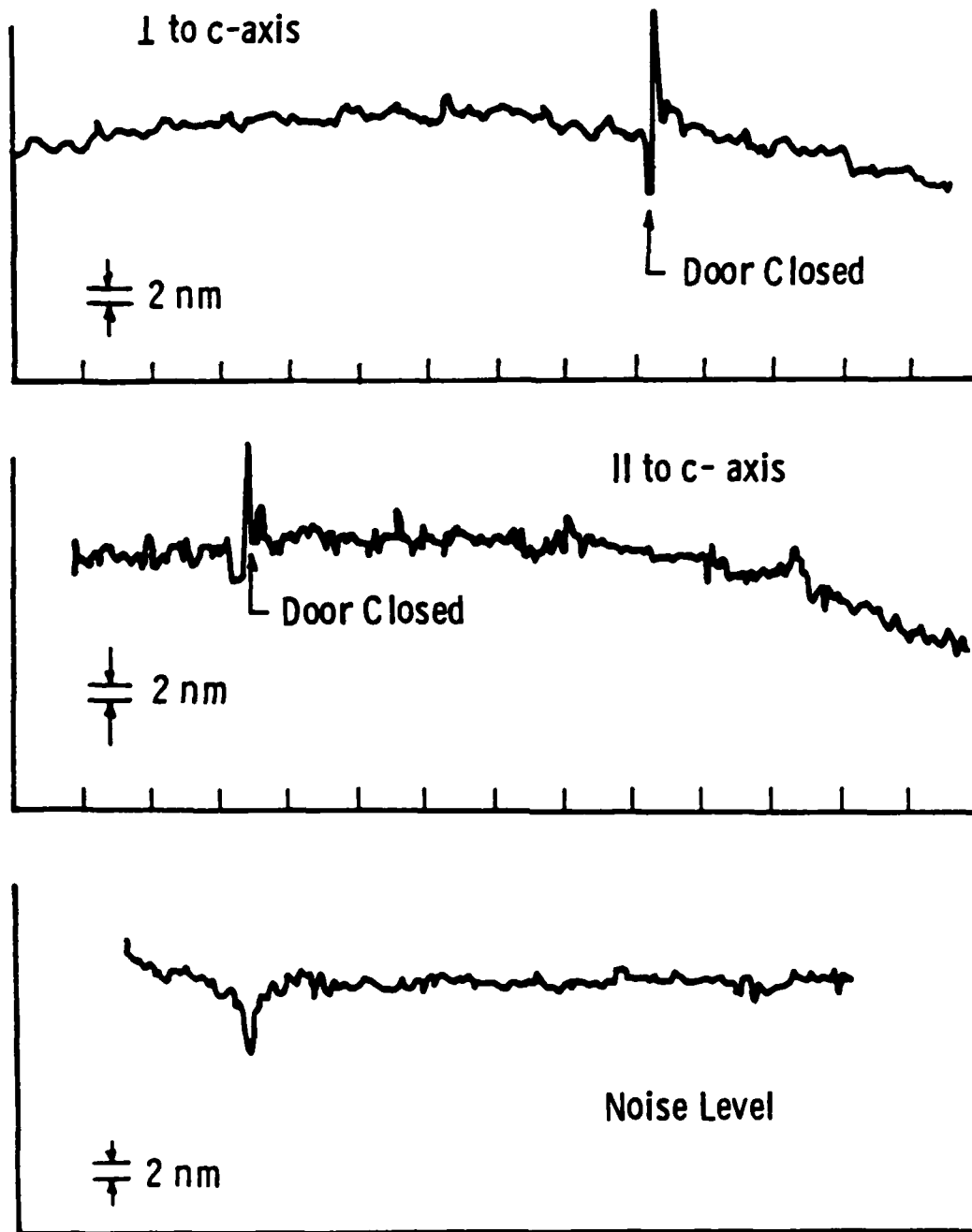


Figure 46. Talystep traces on W98 in different directions relative to c-axis projections.



A

B

C

D

E

A. Silicon wafer

B, C. Vendor wafers

D, E. Low temperature wafers

10 microns

Figure 47. Nomarski differential interference constrast micrographs at 2000 X.

Examination of a stripe pattern defined in aluminum evaporated onto a silicon wafer shows that the stripe edges become dark for a particular rotation angle. A further 90° rotation of the stripe pattern sample brings the stripe edges to a maximum brightness. The reason for a single maximum of brightness for the SOS wafer is not understood.

Figure 47 also shows views of Westinghouse epilayers. The granularity is more pronounced and somewhat coarser. This is consistent with the greater haze measured on these wafers. There is no obvious pattern in the surface texture that would explain the four-fold symmetry of rotation angle scattering of the Westinghouse wafers, as compared to the two-fold symmetry of the vendor wafers.

In summary, we have shown that the UV scattering haze is caused by the surface topography of the silicon epilayer. Metallized sapphire substrates do not show the characteristic scattering peaks, so we conclude that the roughness of the silicon surface is not simply a replication of the substrate surface. The surface texture can also be observed by Talystep and Nomarski methods.

At this time, there is no completely consistent picture available for the cause of the UV scattering peaks. Further discussion appears in Section 4.1 and in the Conclusions.

4. ADDITIONAL CHARACTERIZATION

4.1 Cross-Section Transmission Electron Microscopy (XTEM)

The UV scattering haze measurements showed a wide variation in haze levels among wafers prepared in different ways. Rotation angle scans of the scattering from SOS wafers, metallized wafers, and metallized substrates showed that the scattering is due to the texture of the silicon surface, and that this texture is crystallographically oriented with respect to the substrate. Attempts to directly observe the surface texture by optical microscopy and profilometry were inconclusive. Attempts were also made to produce replicas of the surface for TEM examination. The replicas were not useful because the surface relief was too small to show up well in the conventional method of shadowing by low-angle evaporation.

The definitive method for observation of crystal defects is transmission electron microscopy. This method was employed to examine cross sections of silicon epilayers. The objective was to observe directly whether crystal defects give rise to surface asperities that could cause scattering.

4.1.1 XTEM Technique

The SOS wafer is lapped by a deposited layer of SiO_2 (Silox) to protect the silicon surface and to provide an easily distinguishable surface boundary. The wafer is scribed using a Nd:YAG laser to generate overlapping damage spots on the surface of the epilayer. The scribe lines divide the wafer into 2 mm squares. Before breaking the wafer, each square is marked with an indelible marker to preserve the orientation of the sample. The wafer is broken into individual square chips. The chips are glued together with a low-viscosity epoxy to form

a cube about 2 mm on edge, as shown in Figure 48. Care is taken to align the chips with respect to the reference mark, and to preserve the orientation of the glued block during subsequent thinning and mounting for microscopy. The cube is then mechanically ground to $< 75 \mu\text{m}$ in thickness to form the configuration shown in Figure 48b. Further thinning of this specimen is accomplished by ion milling until a small perforation appears in the specimen. This perforation must appear near one of the $\text{SiO}_2/\text{Si}/\text{sapphire}$ layers to produce a thin tapered section of $\approx 500\text{-}1500 \text{ \AA}$ in thickness suitable for TEM studies. The specimen preparation is time consuming, and care must be exercised at every step to avoid damage of the brittle specimen. SOS has the advantage of being fairly mechanically stable; however, the large differential in milling rates between Si and sapphire necessitates that the mechanically thin specimen be $< 75 \mu\text{m}$ before ion milling.

The ion milling was accomplished in a GATAN dual ion mill using Ar ions at 6 kV and $\approx 15^\circ$ milling angle. The specimens were examined in a Philips 400T TEM/STEM operating at 120 kV.

4.1.1.1 TEM Defect Analysis of Microtwins in SOS

The main crystalline defect which was to be analyzed by TEM was microtwins in the Si layer. In order to ensure that the microtwins would be visible, the TEM specimens were prepared such that the electron beam would travel along one of the $\langle 110 \rangle$ directions of the Si layer. This is a special orientation which allows observation of two sets of the possible four sets of microtwins which generally lie on $\{111\}$ planes in FCC materials.

Figure 49 is a schematic of an electron diffraction pattern obtained in the diamond-type silicon structure when the electron beam is traveling along the $[0\bar{1}1]$ direction; that is, the thin section of the specimen is the $(0\bar{1}1)$ plane perpendicular to the $[0\bar{1}1]$ direction. The spots represent diffracted beam, and the planes which give rise to each diffracted beam are indicated. The X's mark reflections which are

Dwg. 93 57A93

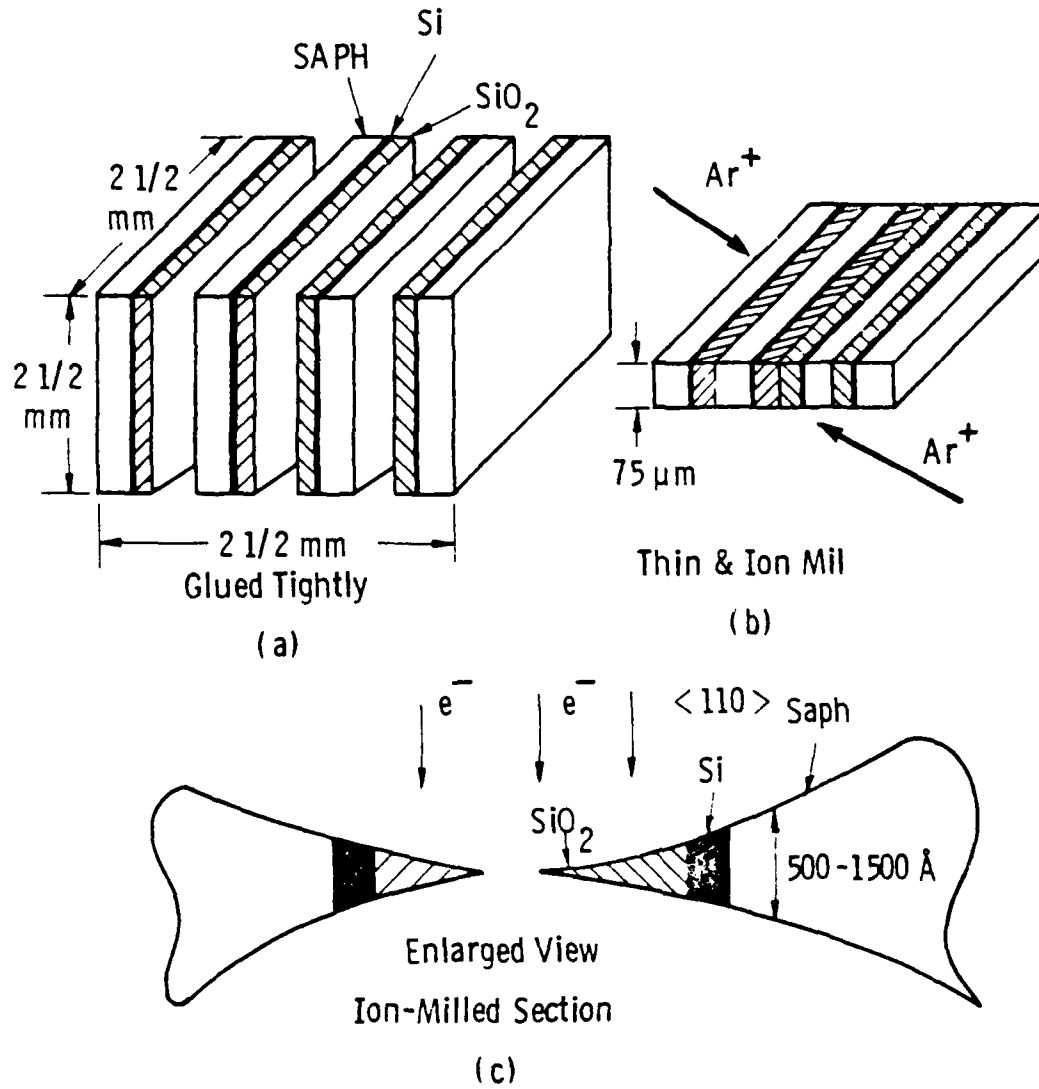


Figure 48. Schematic illustrating procedure for preparing cross-sectional TEM specimens of silicon on sapphire.

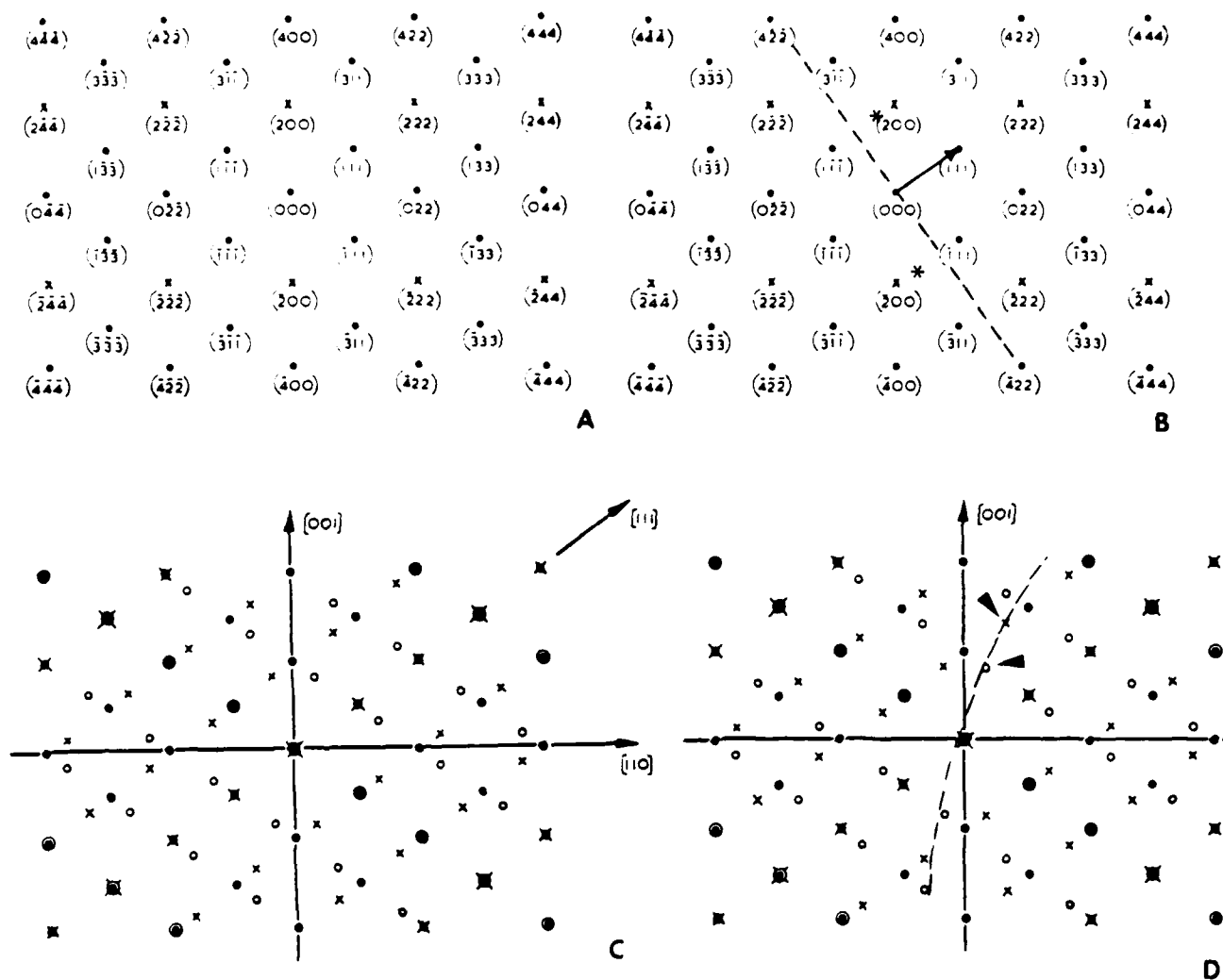


Figure 49. a) Schematic showing electron diffraction pattern of a $\langle 110 \rangle$ zone in diamond-type silicon crystal. b) Same pattern as in a) showing location of (111) twinning plane and two twin spots (asterisks) formed by reflection through the twinning plane. c) Same pattern as in a) showing all possible parent crystal and twin diffraction spots; filled circles are parent crystal, open circle one set of twin reflections, X's second set of twin reflections. d) Arc of strong diffraction spots caused by tilting crystal slightly off axis; two strong twin spots are indicated.

unallowed for the diamond cubic structure but which occur in electron diffraction due to strong dynamical effects such as multiple diffraction. Since the wavelength of the electron is extremely small in electron diffraction, the planes which give rise to each diffracted beam are essentially vertical; that is, parallel to the electron beam and perpendicular to a vector drawn from the origin of the pattern to each reflection. Thus, the (111) plane, which is a possible twinning plane, would intersect the pattern along the dotted line as shown in Figure 49b. Note that two independent sets of {111} planes can be located in this orientation: the (111) plane which is shown and the (1 $\bar{1}\bar{1}$) plane which could be located in a similar manner.

With this background, it is an easy matter to identify the presence of twins lying on either of these {111} planes. Since crystallographically a twin is related to the parent crystal by a reflection of the structure through the twinning plane ({111} planes in this instance), the positions of the twin diffraction spots can be located by a reflection of the parent diffracted spots through the twinning plane. That is, for a twin lying on a (111) plane, reflection of the (111) beam across the twinning plane produces the asterisk near the (200) spot in Figure 49b, and reflection of the (1 $\bar{1}\bar{1}$) spot produces the asterisk near the (200) spot. If this procedure is repeated for each of the parent reflections and a similar procedure repeated for twins which lie on the (1 $\bar{1}\bar{1}$) plane, then the diffraction pattern from a crystal containing both sets of twins will look as shown in Figure 49c, where the solid circles represent diffraction spots from the parent crystal, open circles represent diffraction spots from one set of twins, and X's represent diffraction spots from the second set of twins.

This diffraction analysis can be used to show that the defects imaged are twins and on which particular {111} plane the twins are located. The analysis can also be used to establish the proper imaging conditions for viewing the twins. If the crystal is located exactly on one of the $\langle 110 \rangle$ zone axes such that the diffraction pattern looks as in Figure 49c, then both the twins and the parent crystal are diffracting

strongly and the image appears dark. If, however, the crystal is tilted slightly away from the axis, then only an arc of the possible reflections will diffract strongly and, depending on the location of the arc, the twins and parent crystal will be in or out of contrast. If the arc of reflections corresponds to that shown in Figure 49d, then the twins will diffract strongly and appear as dark in the image. This type of image is shown in Figure 50a, simultaneously showing two sets of twins on {111} planes originating at the Si/sapphire interface. The diffraction pattern is shown in Figure 50b, and the arc of strong reflections can be seen. The twin reflections are highly streaked, indicating that some of the microtwins are only a few atom layers thick. Since there are two sets of twins lying on different {111} planes, the streaks extend in different directions for each separate set of twin reflections.

It is often difficult to orient the crystal exactly such that both sets of twins will be imaged clearly and equally over large sections of the Si layer. Also, if the twin density is high, overlapping images can obscure the relative twin densities. This situation can be rectified by forming dark field images which show each set of twins individually. This is accomplished by tilting the incident electron beam such that the particular twin reflection desired is traveling down the optical axis of the microscope and forms the image. Dark field images of each set of twins shown in Figure 50a are shown in Figure 50c and d. The twin reflections used to form the images are arrowed in the diffraction pattern in Figure 50b and for clarity are also arrowed in the schematic of Figure 49d.

The procedures outlined in this section were used to analyze the twin density and distribution in the Si layer. A bright field image was formed first to show both sets of twins over a relatively large length of the layer. Then individual dark field images of each set of twins were formed to show the relative twin densities more clearly.

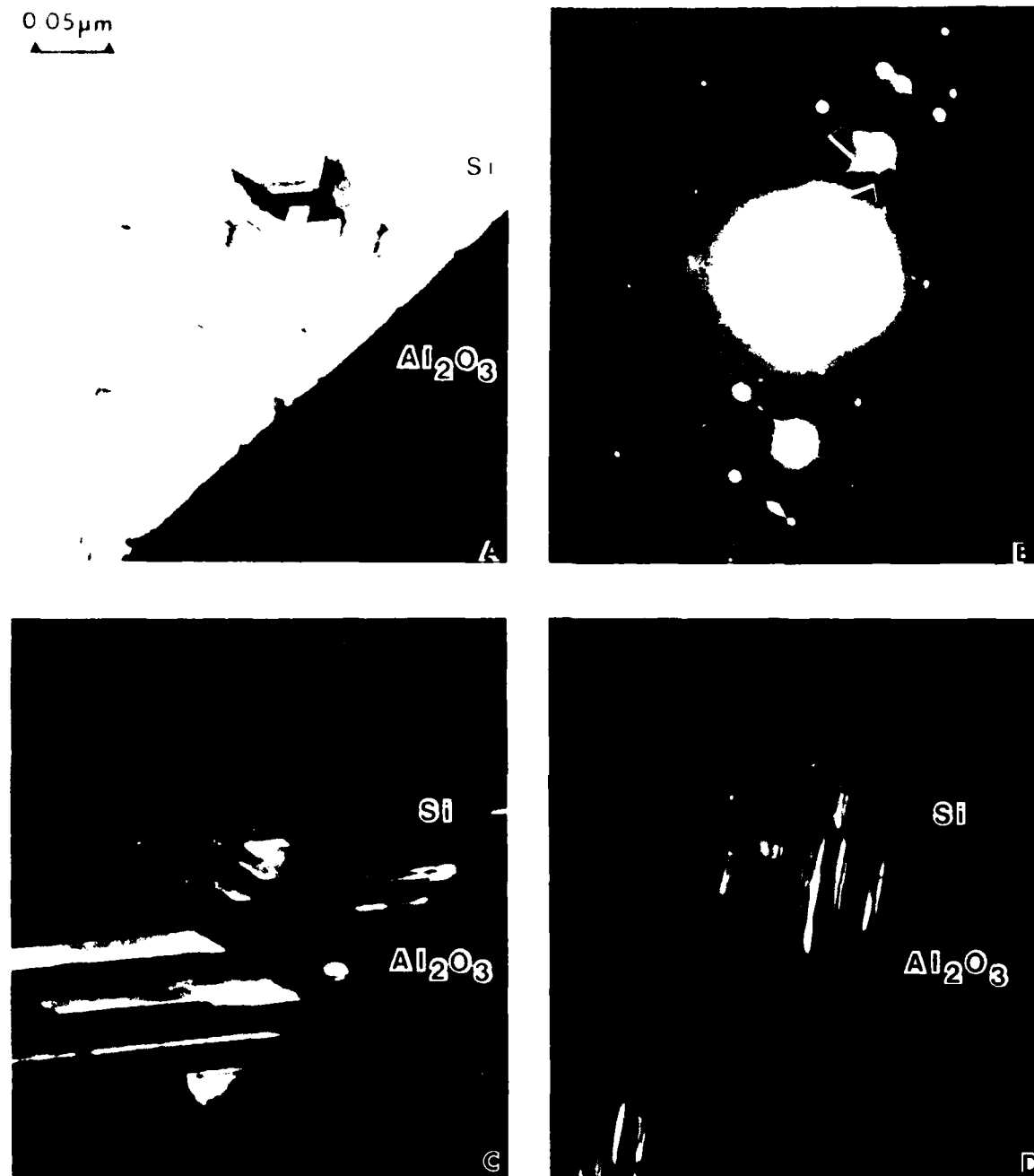


Figure 50. a) Bright field micrograph showing two sets of microtwins in Si imaged under conditions shown in Figure 49b. b) Electron diffraction pattern showing arc of strong reflects; the two twin reflections are indicated. c) and d) Dark field micrographs individually showing each set of twins formed by using twin spots shown in d.

4.1.2 XTEM Results

Several wafers were selected for characterization by XTEM. Because the technique is time-consuming and expensive, it was not possible to investigate the entire range of wafers characterized by UVS haze.

A vendor wafer with high haze is shown in Figure 51. In the bright field view of Figure 51a, all of the twins are visible, while the dark field views of Figure 51b and c show only the twins of selected orientation. The boundary of the silicon epilayer and the Silox covering layer is clearly delineated in the bright field view (Figure 51a). The silicon sapphire interface is seen at the bottom of all three views. Each display is a montage of separate views. The inset of Figure 51d shows the selected area diffraction pattern from this region of the sample. The black rectangles in Figure 51a are the TEM plate identification labels. The viewing direction for Figure 51 is along the 110 axis, as seen in Figure 52. This vendor wafer, W75F, is a Type I wafer, with the c -axis projection located 45° CCW from the flat. The silicon 100 axis is chosen to lie along the c -axis projection. The twin planes that are visible in this orientation are $\bar{1}11$ and $1\bar{1}1$. As Figure 51 clearly shows, the density of twins on the 111 plane is much greater than that on the $1\bar{1}1$ plane. A measure of twin density was obtained by counting the twins observable in the dark field views, at the surface, mid-plane, and silicon sapphire interface. The results are tabulated in Table 10.

Another view of the same wafer is shown in Figure 53. Here, only the dark field views are shown, from a $1\bar{1}0$ viewing direction. The twin density is observed to be greater on the $\bar{1}11$ plane and less on the 111 plane. The densities were counted and entered in Table 10.

A second vendor wafer, W96F, was also prepared for TEM. The resulting cross-section micrograph is shown in Figure 54. This is also



Figure 51. XTEM view of W75F along 110 direction, showing twins on $\bar{1}11$ (majority) and $1\bar{1}1$ (minority) planes.

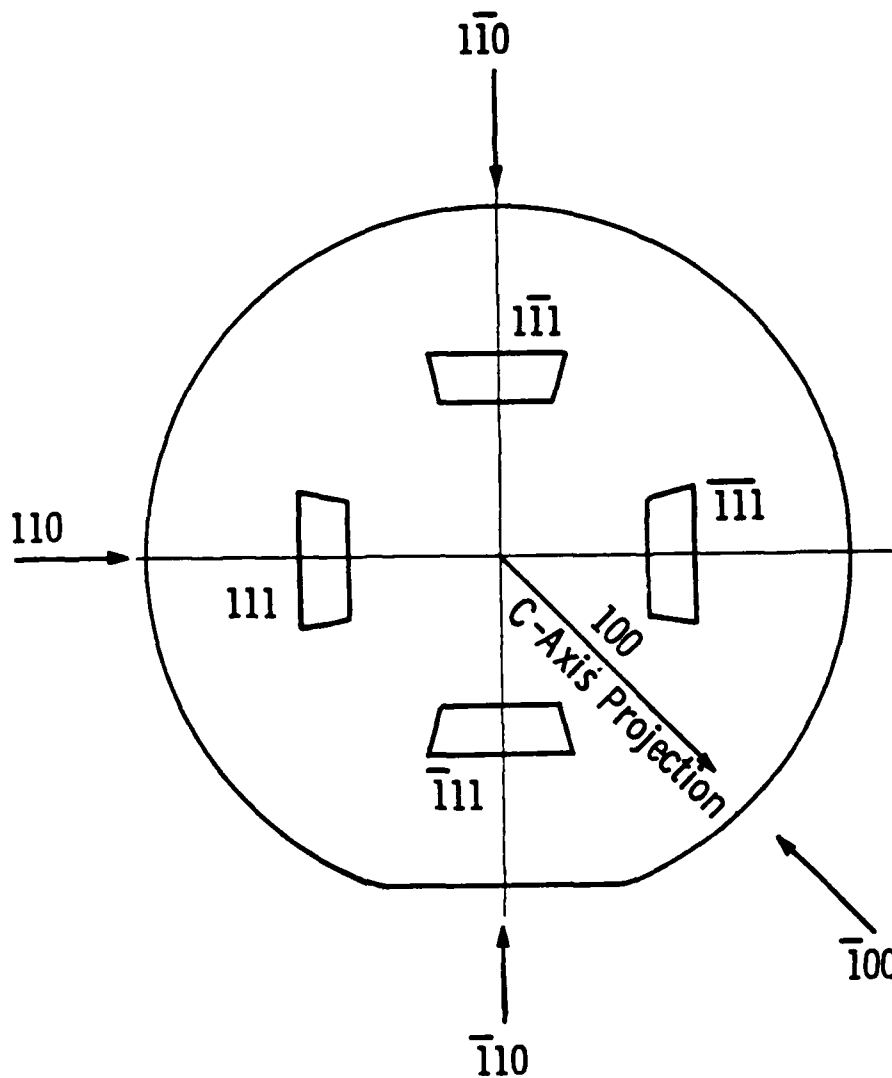


Figure 52. Orientation of twin planes and viewing directions for XTEM views; the silicon (111) planes are shown projecting downward into the epilayer.

Table 10
Twin Densities Determined From XTEM Views

	Twin Density Twins/ μm	W75F	W96F
$\bar{1}\bar{1}1$	Surface	0.3	
	Mid-plane	1.6	
	Interface	39.0	
$\bar{1}\bar{1}\bar{1}$	Surface	6.3	2.1
	Mid-plane	6.0	5.3
	Interface	53.0	61.0
$\bar{1}11$	Surface	12.7	
	Mid-plane	13.3	
	Interface	75.0	
111	Surface	0.7	2.1
	Mid-plane	2.3	3.5
	Interface	47.0	34.0
UVS Haze (Haze Numbers)		193.0	90.0
UVS Angular Scan Contrast Ratio		2.15	1.37

a Type I wafer, but with much lower UVS haze than W75F. The twin density is greatest on the $\bar{1}\bar{1}1$ plane. The density counts are also shown in Table 10.

In general, the data displayed in Table 10 are consistent with the accepted picture of the defect structures in SOS. The density of twins at the interface is very high, but the density decreases rapidly in the overlying epilayer. Our data show that the density of twins observed at the mid-point of the epilayer is only slightly higher than the density of the surface. The distribution of twins on the (111) planes is highly preferential to the $\bar{1}\bar{1}1$ and $\bar{1}11$ planes. This has also been reported in earlier work.⁽⁵⁾

Table 10 also lists the UVS haze numbers and angular scan anisotropy ratios. Wafer W75F has about twice as much haze, while the

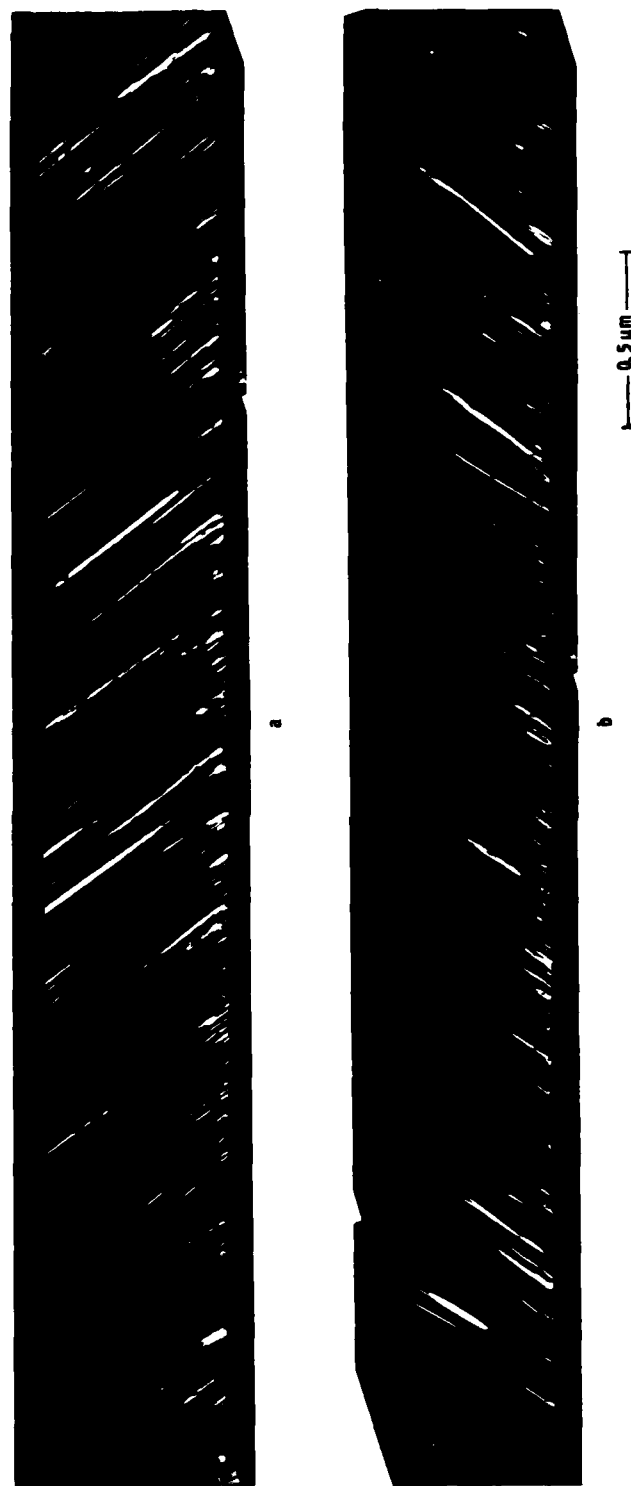


Figure 53. Dark field XTEM views of W75F along 110 direction, showing twins on 111 (majority) and 111 (minority) planes.

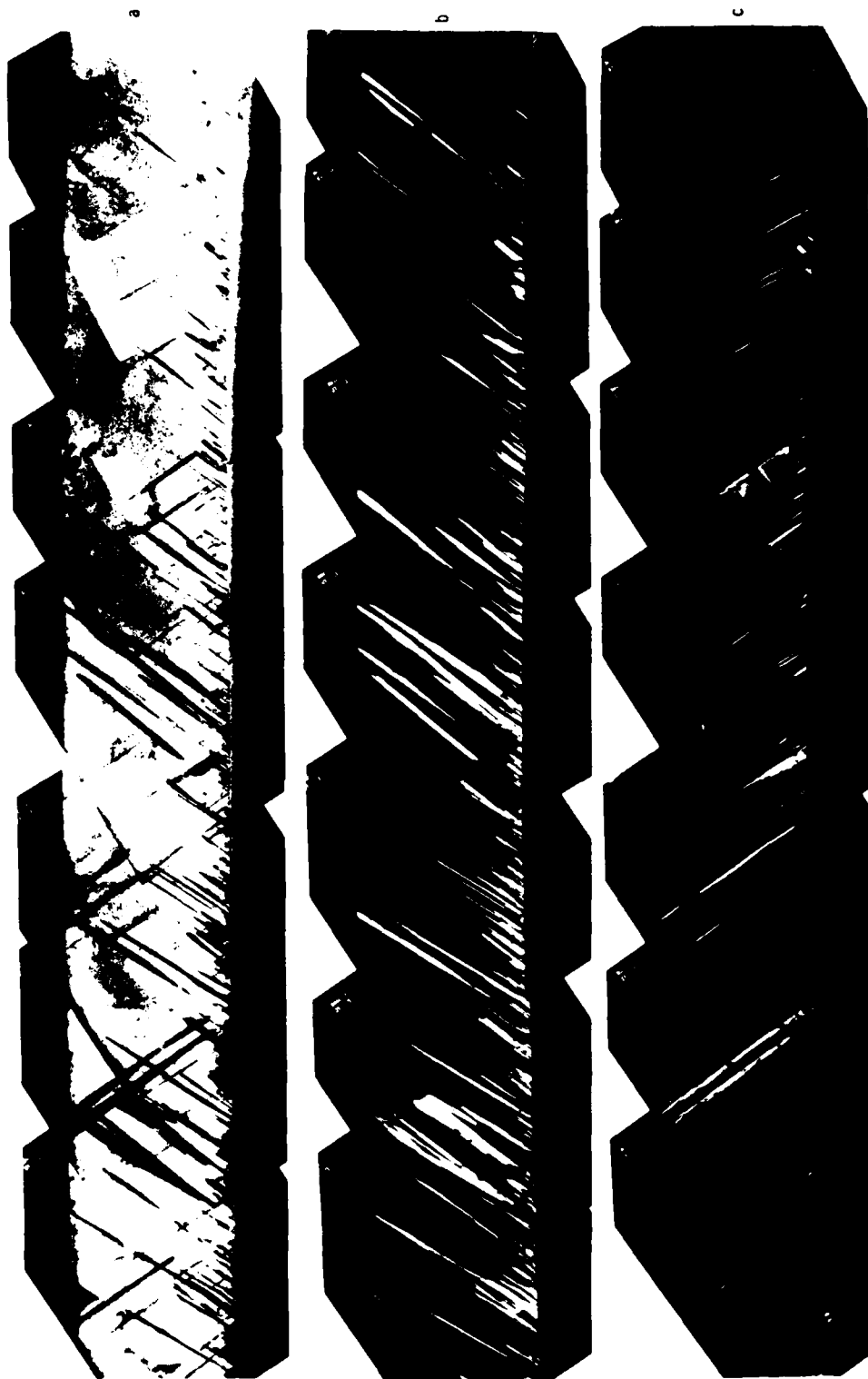


Figure 54. XTEM views of W96F along 110 direction, showing twins on 111 (majority) and 111 (minority) planes.

surface twin density is three to six times as great as W96F. This suggests a positive correlation between UVS haze and defect density. The rotation angle anisotropy for W75F is 2.15, among the highest of all SOS wafers measured, while W96F has a low ratio at 1.37. It is interesting to note that W75F also has a high ratio of surface twin densities on the majority twin planes relative to the minority planes, while W96F has approximately equal twin densities of these planes. A sample of two wafers is obviously too small to establish these relationships on any statistical basis. We turn next to an examination of causal relationships.

It was established by metallizing the SOS wafer surface that UVS haze is due mainly to surface contours. The TEM cross sections were inspected for direct evidence of surface features. Figure 55 shows high-magnification views of regions where twins intersect the surface. Very small surface asperities can be observed on the point where the twin emerges. The amplitude of the asperity is about 5 nm. Another type of surface contour can also be observed by laying a straight edge along the silicon surface of Figures 51, 53, and 54. The surface is most clearly delineated in the bright field views. Surface contours about 5 nm in amplitude with a length of 100 to 200 nm have been found. Some of these contours, which are typically smooth, shallow depressions in the surface, are found near twins. However, other surface troughs are not near any twins. Surface features of sizes larger than about one micrometer in extent would be difficult to find due to the problem in precisely registering the successive photos in the montage views. Attempts to get a more comprehensive view of the surface texture by making a surface replica were unsuccessful, as the replicas showed very little contrast. Talystep traces, with lateral resolution limited to about 12 μ m by the stylus diameter, showed surface contouring of 2-3 nm. Piecing together the information on hand, we can begin to see which features can contribute to UVS haze. First, the very small surface asperities on the twin traces on the surface are not likely to cause the observed scattering. The characteristic UVS peaks in rotation

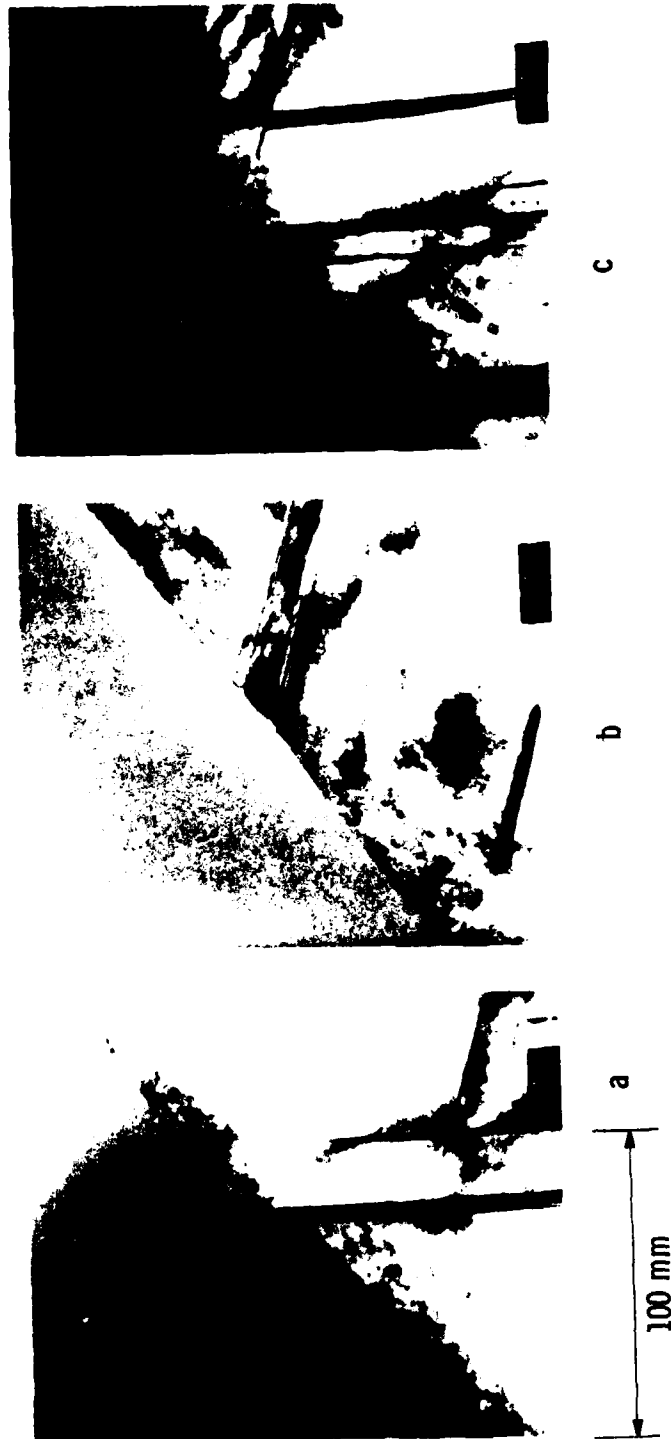


Figure 55. XTEM views of surface asperities where twin planes intersect surface.

angle scans are observed to persist when the SOS wafer is coated with up to 100 nm of metal. The sharp asperities where the twins emerge will be smoothed over by the deposited metal. In addition, the twin traces lie on the surface at 45° angles with respect to the c-axis projection. Linear features so aligned should give peak scattering at right angles to their linear axes, or at 45° angles from the c-axis. However, in all cases, the scattering peaks are observed at 90° angles from the c-axis. This symmetry property raises difficulties in any hypothesis that relates the UV scattering directly to the twin density. It is necessary to consider whether the twin structure can give rise by an indirect process to surface contours aligned along the c-axis.

Some evidence for extended structures involving more than one twin is shown in Figure 56. In this micrograph, the viewing direction is $\overline{100}$, and both sets of majority twins on the $\overline{111}$ and $11\overline{1}$ planes are visible. At several places in the figure, there are intersecting twin planes at the middle of the epilayer or higher. Such extended defects presumably extend to the surface, according to the density counts of Table 10. Intersecting twin planes of this type cannot be seen in Figures 51, 53, or 54 because one of the planes would be out of contrast. The existence of intersecting twins, or chains of intersecting twins, can be expected to give rise to more complex surface contours than isolated twins. However, at this point, it is not possible to establish a causal relationship between the crystal defect structure and the surface contours which give rise to UVS haze.

4.2 Current DLTS Measurements on SOS Transistors

Deep-Level Transient Spectroscopy (DLTS) measurements are useful in characterizing traps in semiconductors, including the trap density, energy level, and capture cross section. The most common approach to DLTS measurements is to measure the capacitance associated with the depletion region of a Schottky-barrier diode or p-n junction diode under reverse bias.⁽²⁹⁾ In such a measurement, the depletion region of the reverse-biased diode is partially collapsed by a pulse which momentarily



Figure 56. XTEM views of W88F along T00 directions showing both majority sets of twins: a) bright field view showing extended defect structures, b) and c) higher magnification views of two extended defect regions.

reduces the magnitude of the reverse bias. During the time of the pulse, traps in the original depletion region are flooded with carriers, and essentially all of the traps become filled. Immediately after the pulse, the original depletion region is perturbed by the trapped charge, and this changes the capacitance of the depletion region. With time, the trapped charge is emitted and the capacitance associated with the depletion region returns to its steady-state value. The rate at which the trapped charge is released depends on the position of the trap energy level in the semiconductor bandgap and the temperature of the sample. Thus, by observing the capacitance transient associated with the bias pulse and its aftermath, the characteristics of traps which lie within the steady-state depletion region can be determined.

Capacitance DLTS, however, is not well suited for thin layers, such as the silicon layer in an SOS structure, because a reverse bias can cause the depletion region to extend to the substrate with ill-defined consequences. Furthermore, it is frequently the behavior of a fully processed MOSFET that is of primary interest, rather than the characterization of the starting layer. Use of an SOS MOSFET as the test device in a DLTS measurement enables the device itself to be characterized so that processed-induced traps can also be observed. In this case, the depletion region that is collapsed is the depletion region beneath the gate. It is within this restricted region that traps are detected. Hence, the technique is capable of sensing traps with a high degree of spatial resolution, with the area sensed given by the area of the gate.

In implementing the DLTS technique with a MOSFET as the test device, it is the drain current which exhibits the transient behavior after a bias pulse is applied to the gate. This is because charge which is trapped during the bias pulse remains in the depletion region after the bias pulse and alters the threshold voltage of the MOSFET. As the traps release their captured charge with time, the threshold voltage changes. Since the gate voltage is constant at all times except during the pulse, a changing threshold voltage means a changing drain

current. Assuming that the concentration of trapped charge decreases exponentially with time, it follows that the drain current likewise changes exponentially with time after the gate bias pulse. These ideas are developed quantitatively elsewhere.⁽³⁰⁾

A schematic diagram of the current DLTS set-up and the current transient that is produced is given in Figure 57. The devices studied in this work are n-channel enhancement-mode MOSFETs. Consequently, in steady-state operation a positive voltage (~ 2.0 V) is applied to the gate so that a small current (~ 10 μ A) flows from drain to source under the influence of a modest voltage between drain and source (~ 50 mV). The gate is pulsed to zero volts, thereby dissipating the conducting channel and collapsing the depletion region beneath the gate. During this time, majority carriers (holes) fill the traps in the region where the depletion field has collapsed. Note that only majority carrier traps can be sensed by this technique, since only majority carriers are available to flood the depletion region. During the time of the pulse, the drain current is reduced to zero. Immediately after the pulse the drain current exceeds the steady-state value because the trapped holes (positive charge) partially offset the ionized acceptors (negative charge). In this condition the doping density is reduced, in effect, and with it the threshold voltage is reduced. The excess current which flows as a result decays to zero as the traps emit their captured holes, as illustrated in Figure 57. The drain current is converted to a voltage, amplified, digitized, and sent to a computer for analysis.

The system for acquiring and analyzing current DLTS data is shown in block diagram form in Figure 58. The system is controlled by a Digital Equipment Corporation MINC computer with a PDP 11/23 central processing unit. The computer generates the synchronization signal which triggers the pulse generator and timing instruments, and receives the digitized current transient from the current amplifier. The current transient is digitized by a fast (100 kHz) 12-bit A/D converter upon receipt of a trigger pulse from the time base generator. The interval between successive pulses increases exponentially to match the

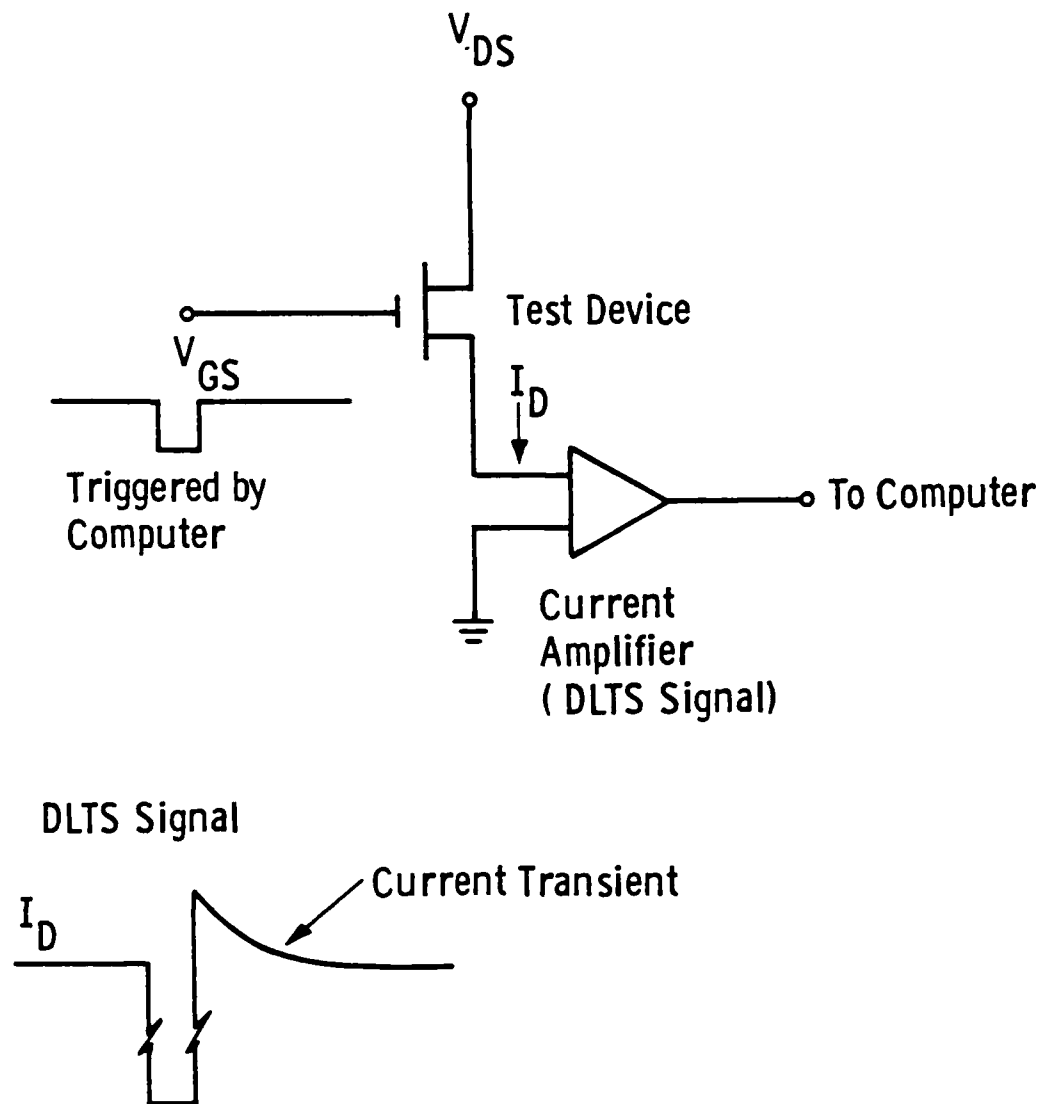


Figure 57. Current DLTS set-up.

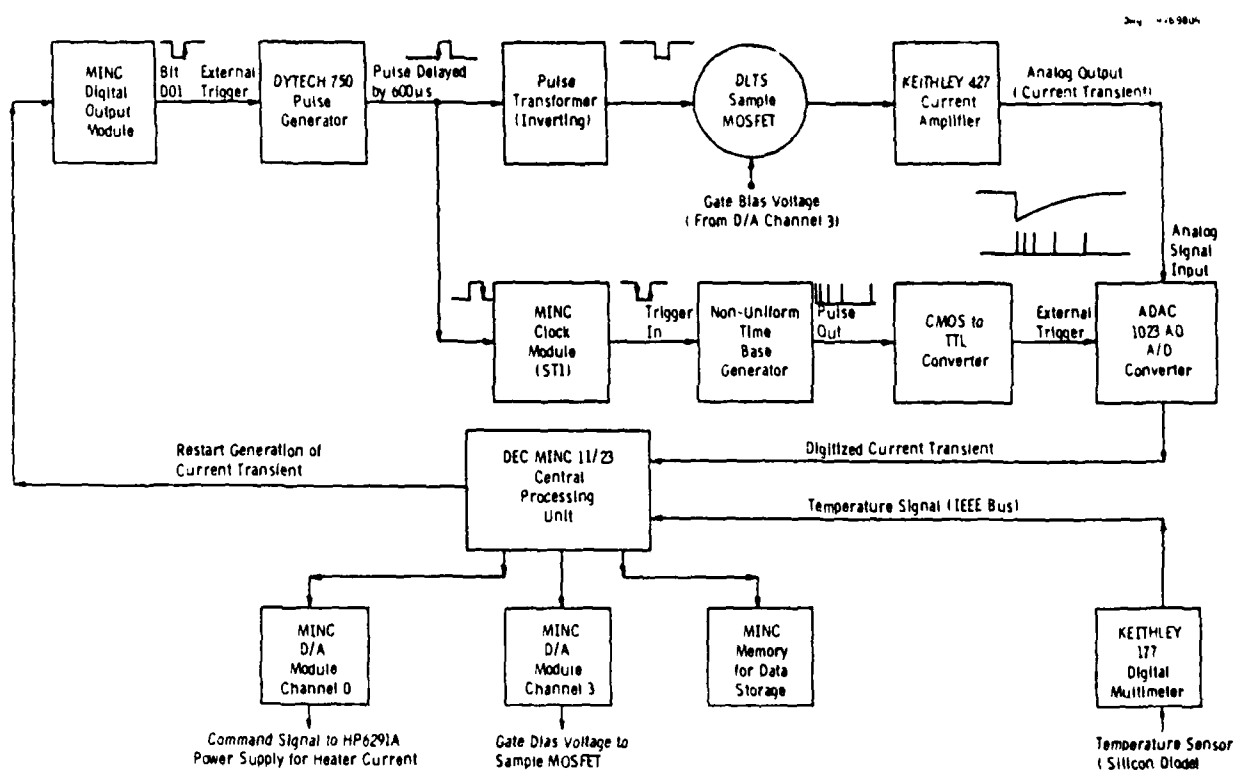


Figure 58. Block diagram of automated current DLTS system.

exponential decay of the current transient. The transient is typically digitized at nine points, with the interval between pulses varying from 100 μ s near the beginning of the transient to 13 ms near the end.

The sample is cooled to $\sim 40^\circ\text{K}$ with a helium gas refrigerator, and then is gradually warmed to room temperature as DLTS data are acquired. The sample temperature is measured with a silicon diode sensor which is read by a multimeter and interfaced to the computer by the IEEE-488 bus. In order to improve the signal-to-noise ratio, ~ 300 transients are acquired and averaged while the temperature increases by $\sim 1^\circ\text{K}$.

The structure and doping densities of SOS MOSFET test devices used in this study are shown in Figure 59. Note that the gate length and width are 2 μm and 40 μm , respectively, so the total area being sensed in the current DLTS measurement is only 80 μm^2 .

The drain characteristics of SOS MOSFET 5425-7-7-6, used as a DLTS test device, are shown in Figure 60. The curves are shown both with the drain current saturated (60a) and with the drain current increasing linearly with drain voltage (60b). The current DLTS measurement is made with the MOSFET biased in the linear region of Figure 60b, and typical bias conditions are $V_{\text{DS}} = 50 \text{ mV}$ and $V_{\text{GS}} = 2.0 \text{ V}$.

Current DLTS measurements were made on several SOS MOSFETs. In some test devices, a peak associated with a hole trap was observed, while in other devices no peak was observed. A plot of a single DLTS peak for sample 5425-7-7-6 is given in Figure 61. This peak was constructed by taking the difference between the value of drain current at 1.54 ms after the bias pulse and the value of drain current at 3.12 ms after the bias pulse, and plotting this difference as a function of temperature. The current axis of Figure 61 is in arbitrary units, but with known instrument settings the peak height indicates that the amplitude of the current transient immediately after the bias pulse is $2.7 \times 10^{-8} \text{ A}$.

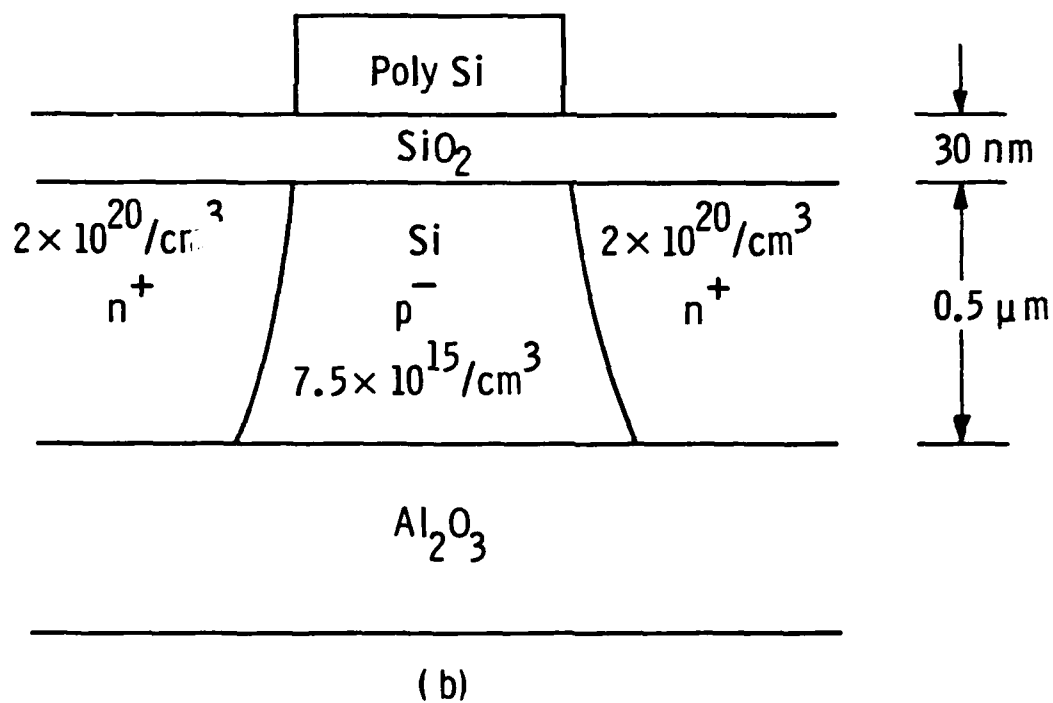
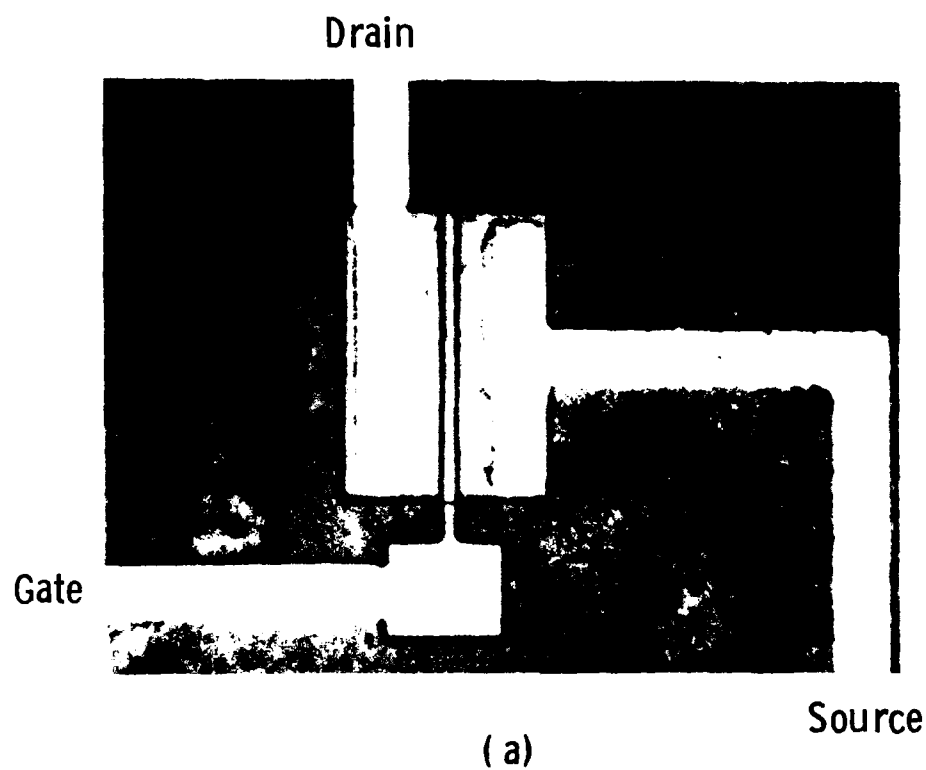
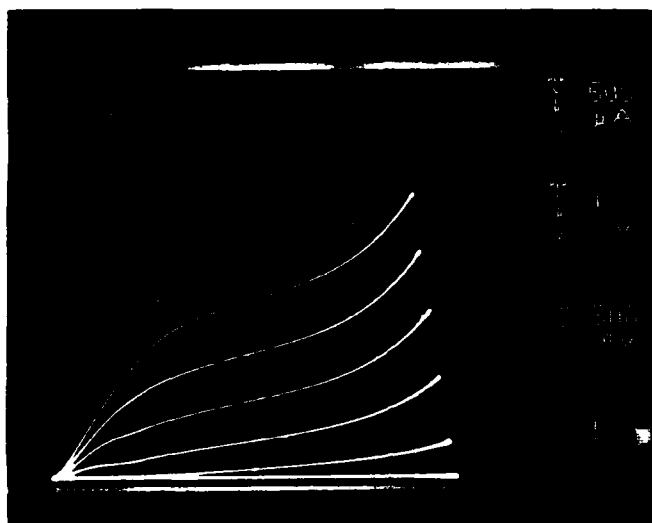


Figure 59. Structure of SOS MOSFET: a) top view, b) cross section. The gate length is 2 μm and width is 40 μm.



(a)



(b)

Figure 60. I-V characteristics of SOS MOSFET (5425-7-7-L) used as DLTS test device: a) drain current saturated, b) drain current varying linearly with drain voltage. Current DLTS measurements are made with the MOSFET biased in the linear region, as in (b).

Curve 746415-A

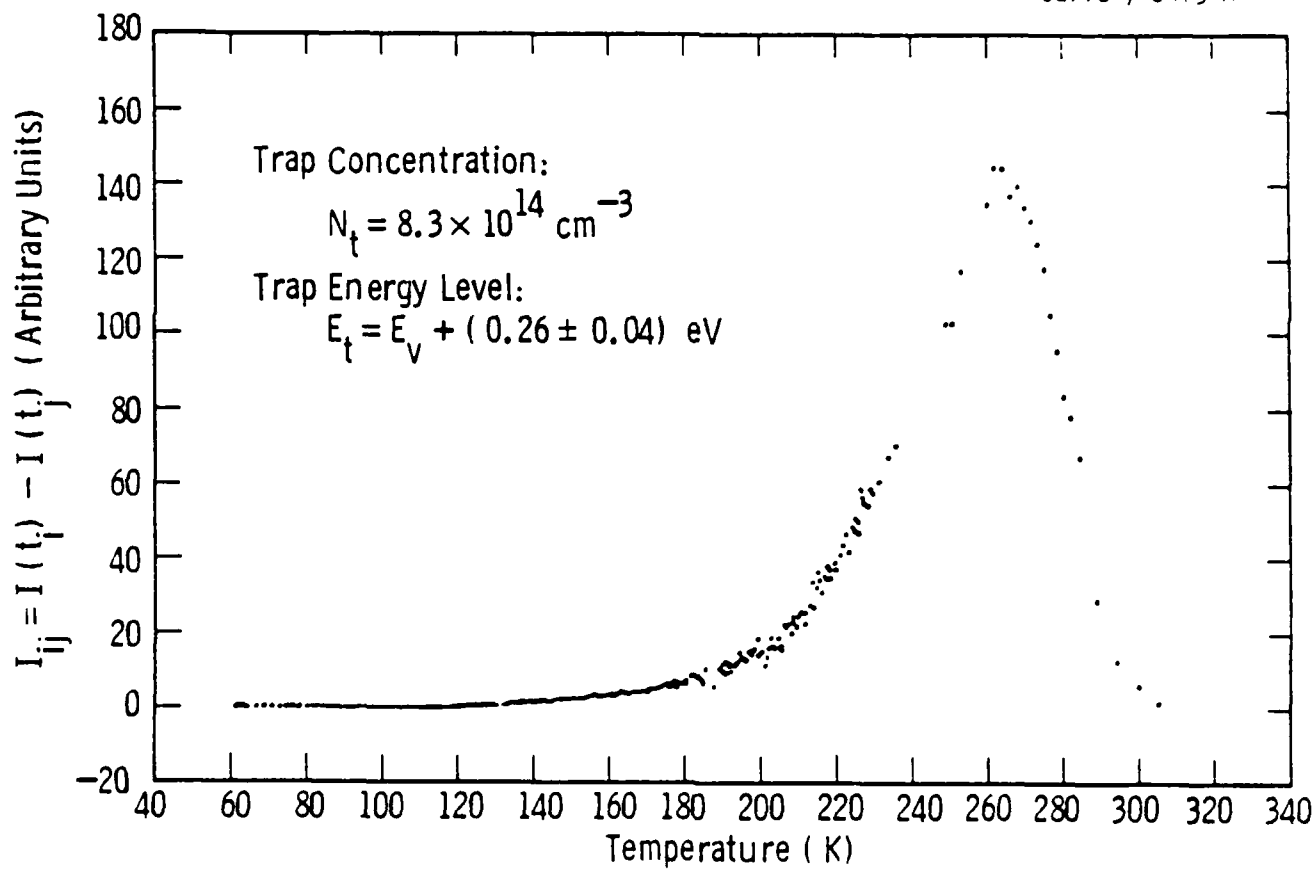


Figure 61. Sample exhibiting peak in current DLTS measurement: SOS chip 5425-7-7, transistor L, $V_{DS} = 50.8 \text{ mV}$, $V_{GS} = 2.00 \text{ V}$.

By examining the value of drain current at other discrete times after the bias pulse (times at which the current transient was digitized), curves similar to that shown in Figure 61 can be constructed. Each of these curves has a peak at a unique temperature. Using a standard technique for analyzing DLTS data,⁽²⁹⁾ the energy level of the hole trap can be determined. In this case:

$$E_t = E_v + (0.26 \pm 0.04) \text{ eV} \quad (5)$$

The expression for calculating the trap concentration relative to the doping density in the silicon beneath the gate is given as⁽³⁰⁾:

$$\frac{N_t}{N_A} = \frac{\Delta I_D(t=0)}{I_D(t \rightarrow \infty)} \frac{2 C_o}{(Q_B / (V_{GS} - V_T))} \quad (6)$$

where N_t is the trap density, N_A is the acceptor doping in the region beneath the gate, $I_D(t=0)$ is the steady-state drain current, $I_D(t=0)$ is the amplitude of the current transient immediately after the bias pulse, C_o is the gate oxide capacitance per unit area, V_T is the threshold voltage, V_{GS} is the steady-state gate voltage, and Q_B is the charge uncovered in the depletion region per unit area at the onset of inversion. Q_B , in turn, is expressed as⁽³⁰⁾:

$$Q_B = - (4 K_{Si} \epsilon_o q \phi_f N_A)^{1/2}, \quad (7)$$

where K_{Si} is the dielectric constant of silicon, ϵ_o is the permittivity of free space, and ϕ_f is the magnitude of the difference between the intrinsic potential and the Fermi potential. When these quantities are calculated, the concentration of traps for the sample of Figure 61 is determined to be:

$$N_t = 8.3 \times 10^{14} \text{ cm}^{-3}.$$

Note that this concentration of traps is approximately 10% of the concentration of dopant atoms.

In contrast, the current DLTS plot of Figure 62 for sample 71-5-11 shows no indication of traps. In this case only an upper bound on trap concentration can be quoted. If a DLTS peak is to be evident, the peak height must be three times as great as the rms noise. Using this criterion, and the magnitude of the noise of Figure 62, it can be stated that traps in sample 71-5-11 are present only at some value less than $4.2 \times 10^{13} \text{ cm}^{-3}$.

A summary of the current DLTS measurements made on SOS MOSFET test devices is given in Table 11. Because of time constraints, only a limited amount of data related to trap parameters was acquired. For this reason, no serious attempt at correlating device properties with measured trap parameters could be made. However, it is interesting to note that the level of $E_v + 0.30 \text{ eV}$, observed in two samples of Table 11, agrees with one of two levels reported for n-channel SOS MOSFETS.⁽³⁰⁾

Table 11
Results of Current DLTS Measurements

Test Device: SOS n-Channel Enhancement Mode MOSFET, 2 μm gate length,
40 μm gate width, $N_A = 7.5 \times 10^{15} / \text{cm}^3$, $t_{\text{ox}} = 300 \text{ \AA}$

Test Conditions:

Temperature Range: 40 - 300°K
 V_{DS} : 50 mV
 V_{GS} : 2.0 V
Pulse Amplitude : 2.0 V
 I_{D} (typical) : 1.0 μA (at room temperature)

Sample	Trap Energy Level	Trap Concentration
5425-7-7-L	$E_v + (0.26 \pm 0.04) \text{ eV}$	$8.3 \times 10^{14} \text{ cm}^{-3}$
5425-7-7-J	$E_v + (0.03 \pm 0.02)$	8.6×10^{13}
71-1-9	$E_v + (0.09 \pm 0.02)$	3.4×10^{13}
71-1-5	None Detected	$< 4.2 \times 10^{13}$
71-5-11	None Detected	$< 4.2 \times 10^{13}$

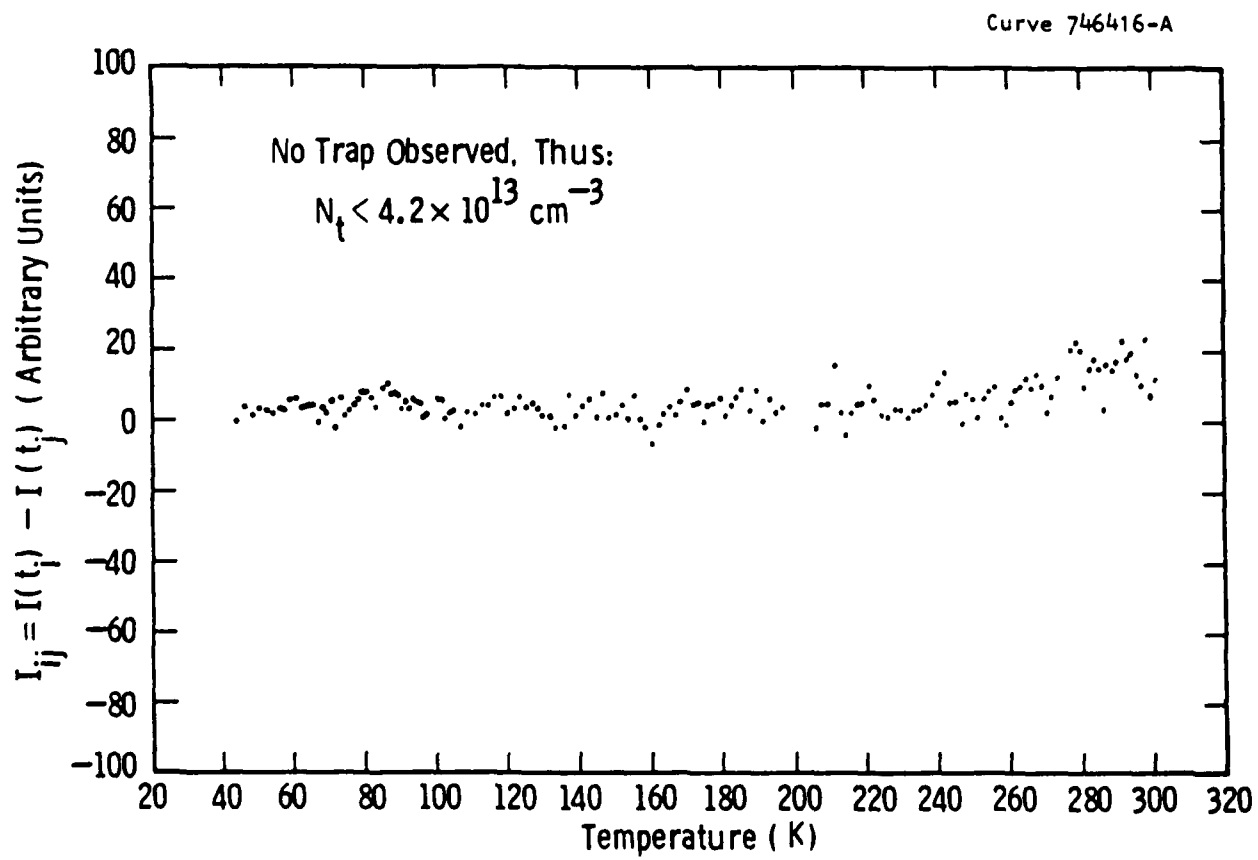


Figure 62. Sample exhibiting no peak in current DLTS measurement: SOS chip 71-5, transistor 11, $V_{DS} = 50.7$ mV, $V_{GS} = 2.0$ V.

5. DEVICE FABRICATION AND TESTING

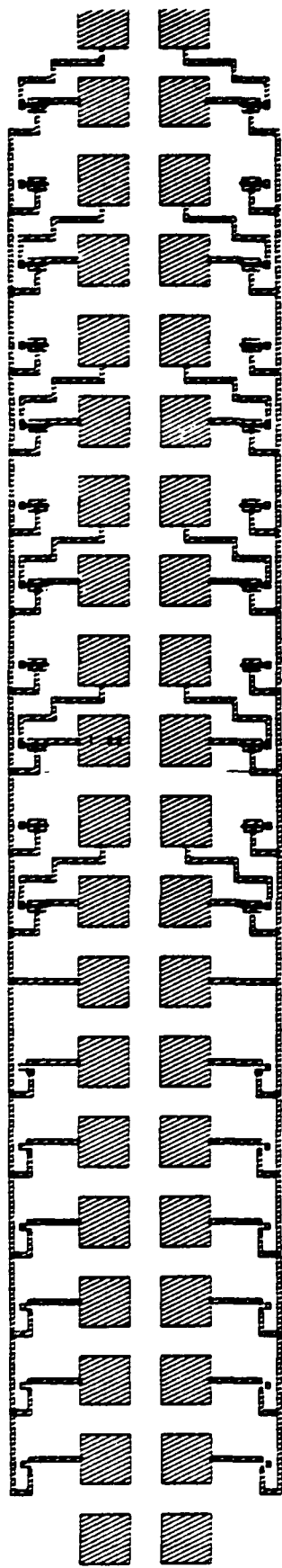
This section describes the fabrication of test vehicles in vendor-supplied and in Westinghouse-grown SOS wafers, as well as the electrical characterization for yield and device performance. Both tasks were carried out at Westinghouse Advanced Technology Laboratories.

5.1 Fabrication Procedure

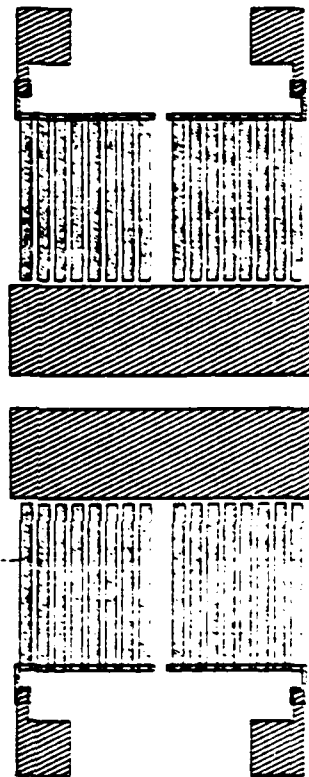
The chosen test vehicle is a modified 4056 VHSIC Phase 0 mask set. Requirements are for at least ten chips having ten identical MOSFETs with individually accessible gate and drain pads. Substrate connections for all devices are left floating.

The original 4056 mask set required modification to the polysilicon and metal levels to fulfill contract requirements for a meaningful statistical analysis. Alterations to the poly level involved the redimensioning of an array of 12 constant-width, variable-length MOSFETs to provide constant-width and constant-length MOSFETs using gate dimensions of 36 and 20 μm , respectively. A CALCOMP plot of the final transistor array is shown in Figure 63.

The metal-layer level required interconnect modifications to allow individual probing of each MOSFET with several gate and drain pads. Originally, several transistors shared the common gate and source contacts, which could present a problem if an interconnect failure occurred. On each wafer there are 20 chip sites with each chip having 12 identical test transistors, all of which were either NMOS or PMOS. Forty 2×2 pads are configured using the NBS standard 160 μm pitch, 100 μm pad with 60 μm spacing. Also used in this study is the large-area capacitor structures (Figure 63b) located in a different quadrant of the mask set. Their area is $3.6 \times 10^{-4} \text{ cm}^2$ with two



(a)



(b)

Figure 63. Calcomp plot of transistor array (a) and large-area capacitor (b).

individual poly plate areas with separate contacts. Substrate contacts are shared between two pads.

The process selected to fabricate the test vehicle provides a choice of either N-channel or P-channel device fabrication. To simplify the process sequence, the threshold and S/D implant mask steps were eliminated.

For the N-channel process (Table 12), only four mask steps are required. Steps 1-6 define silicon island areas. The silox is used to mask the nitride layer when etching in hot H_3PO_4 . Silicon islands are etched in a warm KOH solution, which removes 2.5 μA of epitaxial silicon. Edge leakage is prevented by the use of a BF_2 blanket implant (only in the N-channel process). The nitride mask blocks the island areas from the BF_2 implant.

A 6.5 μA field oxidation is performed to consume the remaining 2.5 μA of silicon followed by a 300 \AA scattering oxidation.

Punchthrough and threshold adjust implants are performed in both NMOS and PMOS processes after which the scattering oxide is stripped and the gate oxide (275 \AA) is regrown. A 200 \AA nitride layer is deposited over the gate oxide to reduce polysilicon-to-substrate shorting. Polysilicon is deposited and doped to 25 ohms per square sheet resistance. The polysilicon gates are then 80% parallel plate plasma etched in CCl_4 gas and 20% chemically etched to provide a selective etch over thin oxide/nitride.

The polysilicon gates are then oxidized, and a 250 \AA nitride layer for S/D implant scattering is deposited. N-channel devices have a double shallow/deep implant at 80 KeV and 190 KeV; P-channels have a single implant at 80 KeV. Silox is deposited and densified. Densification at 900°C for 20 minutes in O_2 also activates the source drain implants.

Contact windows are chemically etched and 8 μA of flash source aluminum is deposited and defined. Etching of aluminum is done

Table 12
NMOS and PMOS Process Description

STEP	DESCRIPTION
1	Wafer Sheet
2	Photo Number
3	Oxidation 300 Å
4	Nitride 2000 Å
5	Silox 1000 Å
6	Photo-Silicon Island Definition 4056-1B
7	Silicon Island Etch
8	Edge Leakage Implant BF_2 $6 \times 10^{12}\text{-cm}^{-2}$ @ 100 KeV
9	Field Oxidation 6000 Å
10	Special Etch (nitride removal)
11	Implant Barrier Oxidation 300 Å
12	P-well Implant
	NMOS-B $5 \times 10^{12}\text{cm}^{-2}$ @ 190 KeV
	NMOS-B $9 \times 10^{11}\text{cm}^{-2}$ @ 60 KeV
	PMOS-P 9×10^{11} @ 190 KeV
	PMOS-B 8×10^{11} @ 50 KeV
13	Anneal 900°C, 30 min
14	Gate Oxide 300 Å
15	Gate Nitride 200 Å
16	Poly Deposition 6000 Å
17	Poly Doping Phos Diffusion to 25
18	Photo Poly Definition 4056-6B
19	Anneal 900°C, 30 min
20	Nitride LPCVD 250 Å
21	Source/Drain Implant
	NMOS-P $1 \times 10^{15}\text{cm}^{-2}$ @ 80 KeV
	NMOS-P $1 \times 10^{13}\text{cm}^{-2}$ @ 180 KeV
	PMOS-BF2 1.4×10^{15} @ 100 KeV
	PMOS-B 1×10^{14} @ 80 KeV
22	Silox Deposition LPCVD 5000 Å
23	Photo-Contact Windows 4056-9A
24	Anneal 900°C, 30 min
25	Al Evaporation Al 8000 Å
26	Photo First Metal 4056-11c
27	Sinter 400°C, 30 min

chemically. Finally, the contacts are sintered at 450°C for 30 min in N₂ ambient.

5.2 Test Method and Data Tabulation

The Keithley models LPT-2 and LPT-300 were used to obtain automated test data. The following parameters were measured for each transistor.

1. Threshold voltage
2. Transconductance
3. Leakage Current (S/D)
4. Mobility

Sample I-V curves are shown for each (Figure 64), illustrating near-standard transistor characteristics. The "KINK" effect is noticeable in NMOS device lots 5425, 5436, and 5457, whereas the PMOS device has near-flat curved saturation behavior. Contact resistance is noticeable in the 5436 sample by the "S"-shaped current trace before saturation.

Threshold voltage was measured by measuring V_{GS} at a specified current level of 1 μ m with gate and drain terminals tied together. The allowable range for this parameter is $0.1 = V_{TH} < 2$ V for N- and P-channel devices.

Using the general equation for transconductance:

$$g_m = \Delta I_{DS} / \Delta V_{GS} \big| V_{DS} \quad (8)$$

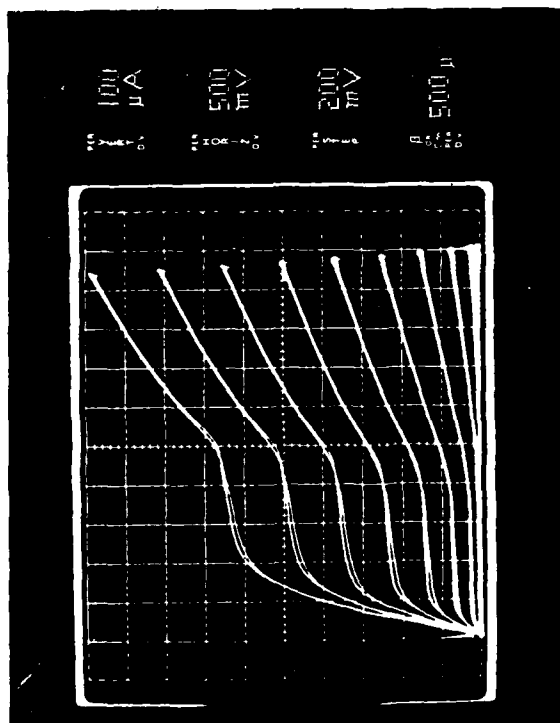
values were obtained for $\Delta V_{GS} = V_{G2} - V_{G1}$ and ΔI_{DS} where:

$$V_{G2} = 5.5 \text{ V,}$$

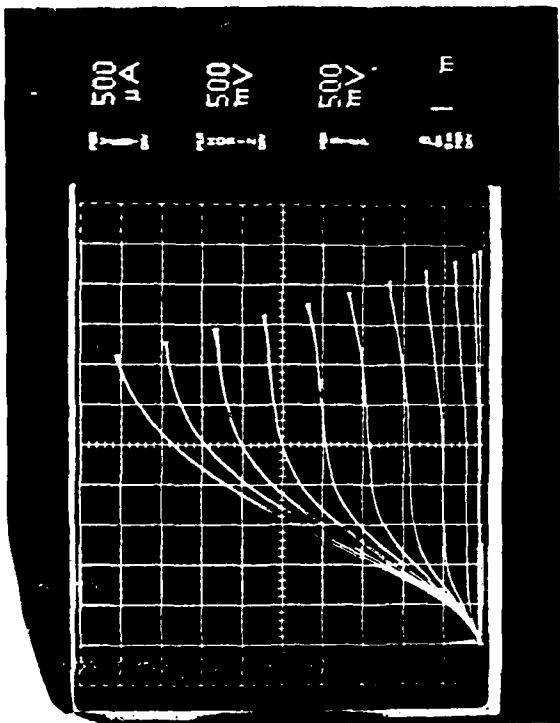
$$V_{G1} = 4.5 \text{ V,}$$

$$V_{DS} = 5.0 \text{ V}$$

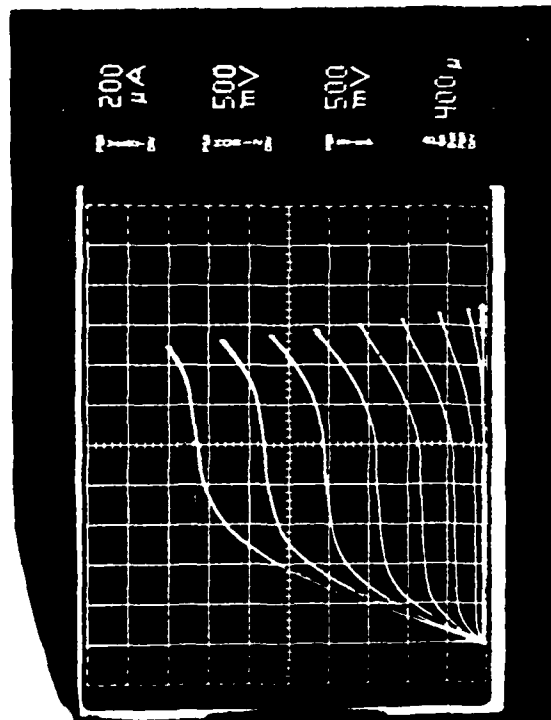
and $\Delta I_{DS} = I_{DS2} - I_{DS1}$ was measured for each bias case.



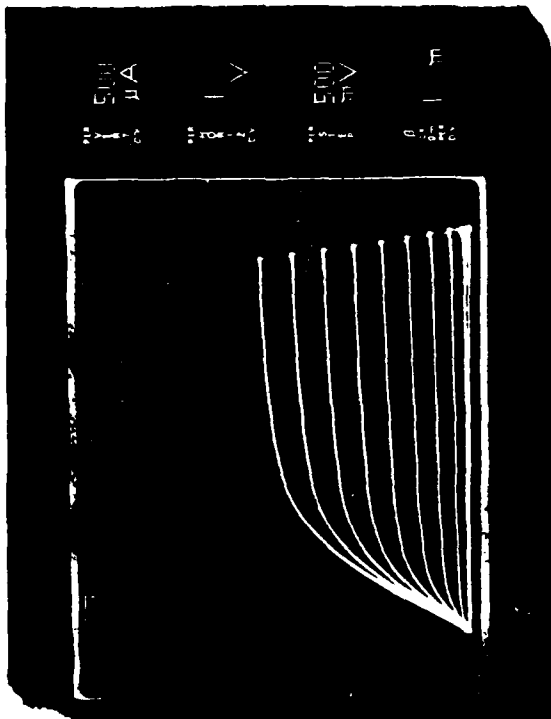
5425-10



5436-11



5457-7



5458-3

Figure 64. Sample I-V Curves.

Upper and lower bounds for μ_m were chosen from .5 mS to 10^8 S for both P- and N-channel devices.

Using a curve fit to the general MOSFET drain current equation in the linear region (i.e., $V_{DS} \approx 50$ mV-100 mV):

$$I_{DS} = (W/L) \mu_o C_i (V_G - V_T) V_{DS} \quad (9)$$

The source drain resistance $R_{DS} = V_{DS}/I_{DS}/V_{GS}$ is measured for two gate-to-source bias levels. Since all other parameters are known, μ_o can be solved for as follows:

$$\mu_o = (L/W) (1/C_i R_{DS} (V_G - V_T))$$

C_i is determined experimentally using C-V measurements for maximum capacitance. Experimental extraction of C_i was done using high-frequency C-V measurements to eliminate complexity caused by the nitride/oxide sandwich dielectric layers. C-V plots were swept from -7 V to +7 V using a bias frequency 1 MHz on an HP9826 automated C-V test station. Insulator capacitance values are listed at the header for each wafer measurement since C-V measurements were done to characterize dielectric properties of each wafer. Mobility bounds were specified from 20 $\text{cm}^2/\text{V-S}$ to 500 $\text{cm}^2/\text{V-S}$. These bounds indicate a properly functioning device.

With the gate terminal grounded and 5 volts applied from drain to source, the drain source current (leakage current) was measured. Bounds for leakage current were specified from 0.0 μA to 10 μA .

All the above parameters were measured for each transistor, averaged for each die site, then averaged for each wafer. Figure 65 shows a sample printout of test data.

At the top, device type (P or N) is specified followed by insulator capacitance, C_i , which is in units of capacitance per unit area (cm^2). Length and width are also listed for each device.

WAFER # 13
 TYPE N
 C= 0.131000E-06 FARADS/CM**2
 L= 2.00 MICRONS
 W=36.00 MICRONS

IDS	VDS	VGS	VBS	
0.111000E-03	0.500000E-01	2.50000	0.000000	A
0.129300E-03	0.500000E-01	3.00000	0.000000	A
0.521750E-05	5.00000	0.000000	0.000000	A
0.540500E-02	5.00000	4.50000	0.000000	A
0.674250E-02	5.00000	5.50000	0.000000	A
0.382900	=Vt A			
444.701	=U1 A			
419.049	=U2 A			
431.875	=U3 A			
0.133750E-02	=GM1 A			
IDS	VDS	VGS	VBS	
0.106200E-03	0.500000E-01	2.50000	0.000000	B
0.125000E-03	0.500000E-01	3.00000	0.000000	B
0.578750E-05	5.00000	0.000000	0.000000	B
0.532000E-02	5.00000	4.50000	0.000000	B
0.664000E-02	5.00000	5.50000	0.000000	B
0.374500	=Vt B			
423.789	=U1 B			
403.217	=U2 B			
413.803	=U3 B			
0.132000E-02	=GM1 B			

CHIP # 12 SUMMARY

	MEAN	STD. DEV.	% PASS
Uo	390.428	10.8674	91.67
Gm	0.132318E-02	0.254865E-04	91.67
Vt	0.625708	0.184672	100.00
IL	0.786364E-06	0.294292E-06	91.67

WAFER # 13 SUMMARY

	MEAN	STD. DEV.	% PASS
Uo	304.099	106.192	54.08
Gm	0.125748E-02	0.266976E-03	51.48
Vt	0.542705	0.326527	56.51
IL	0.100171E-05	0.153607E-05	75.87

Figure 65. Sample printout of test data.

Five columns with I_{DS} , V_{DS} , V_{GS} , and V_{BS} and transistor letter are given for each measurement.

The first two rows are raw data values for mobility. The third row is raw data for leakage current. The last two rows are raw data points for transconductance. Following the data points are calculated values: V_{TH} is threshold; U_1 is $U_0 @ V_{GS} = 2.5$; U_2 is $U_0 @ V_{GS} = 3.0$ V; and U_3 is the average of U_1 and U_2 . G_{m1} is the calculated transconductance. The letter following each value is the transistor ID letter.

After 12 transistor measurements, there is a chip summary of U_0 , G_m , V_{TH} , and I_L giving mean standard deviation and % passed based on specified windows for parameters. Follow 12 chip-scanning sections, there is a wafer summary giving the same statistics for the whole chip of 12 die sites tested. A map of the chip sites is shown in Figure 66.

All bulk control wafers processed were found to have MOSFETs with high source-to-drain leakage currents as shown in Figure 67. This is because the MOSFETs are not isolated from each other on bulk wafers, and blanket S/D and V_{TH} implants were used throughout the process. These wafers can be identified as having high ATD ID numbers. For Lot 5425, bulk-sample ID numbers are greater than 15. For the other lots bulk samples have ID numbers greater than 15.

Run 5436 shows the lowest yield in terms of mobility and functional devices. This can be partially due to process-induced faults such as high contact resistance and damaged channel areas. It is suspected that the epitaxial deposition reactor introduced contaminants when the lots had the 900°C, 30 min anneal. Lots 5425 and 5458 did not have this anneal. Run 5457 had the M1 layer reworked after observing noticeable contact problems after M1 definition. During the second rework, an attempt was made to clean out the contaminated windows using a short silicon etch. This was successful on some wafers, although others were badly damaged and exhibit I-V characteristics as in Figure 68. Contact resistance measurements are performed for all the lots and summarized in Table 13.

Dwg. 9357A51

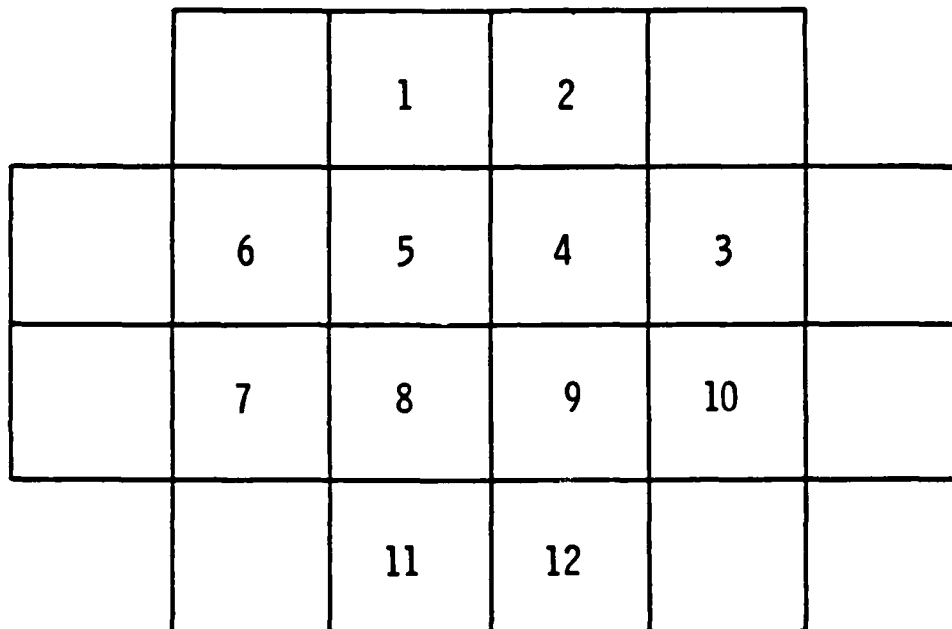


Figure 66. Chip Map.

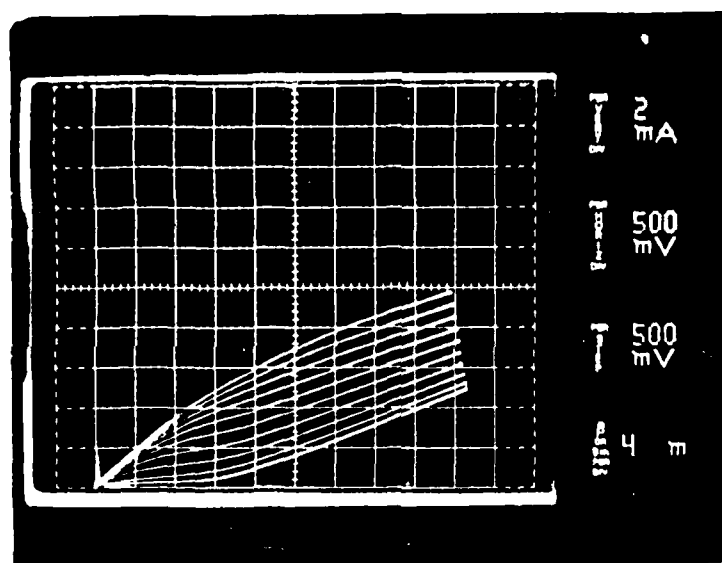


Figure 67. I-V curve showing high source-to-drain current.

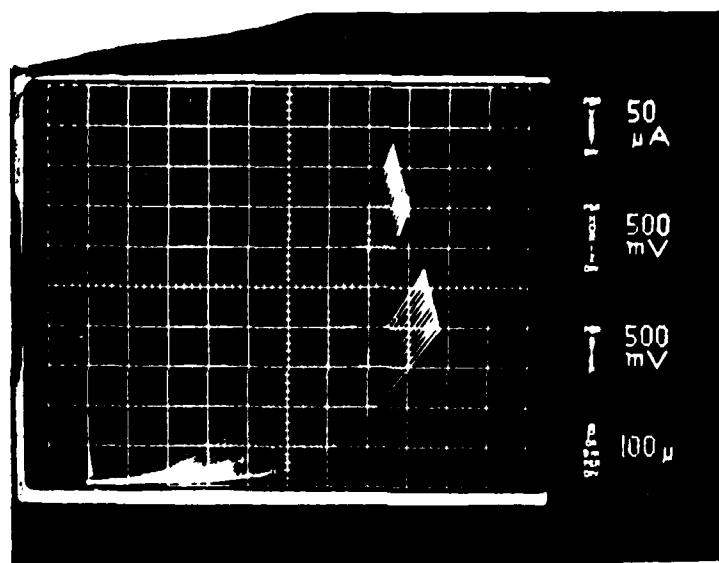


Figure 68. I-V curve showing damage resulting from short silicon etch.

Table 13
Summary of Contact Resistance Measurements

lot	R_c ($\Omega/\mu\text{m}^2$)	δ rms
5425	3.1	0.2
5436	63.4	10.3
5457	10.0	1.5
5458	12.7	6.0

Rather than risk damaging devices in 5636, the first metal level was not reworked. Contact resistance varies by almost a factor of six between 5436 and 5457. The raw data indicate that most devices had extremely low current levels at 50 mV drain-to-source bias, which is probably below the capabilities of the current-measuring instruments.

The target gate oxide thickness is 275 Å. During runs 5636 and 5657 some problems were experienced in obtaining correct oxide thickness, and test runs were performed. However, the lot oxide thicknesses were inconsistent with the test runs. Rather than strip and regrow gate oxide, a process which disturbs underlying threshold implant impurity distribution, the original oxide layers were left intact.

Presented in this section are measurement results from the SOS samples processed at Westinghouse ATL. The raw data are recorded on disk format because the printout data are numerous in content. This section should serve as a guide to interpreting the transistor measurement data so that further analysis can be performed on statistical correlation with characterization results.

6. STATISTICAL ANALYSIS

In this section the device test data and wafer characterization data are analyzed to find statistically significant indicators for device yield and performance. The handling of the electrical test data is described, and processing yield factors are discussed. The statistical correlations of device parameters and characterization numbers are given and their significance is discussed.

6.1 Device Fabrication and Electrical Testing

Four separate fabrication runs were submitted to ATL for device fabrication and wafer testing. The wafers in each run were selected to include high, medium, and low haze, and both vendor and Westinghouse-grown epilayers. Of a total of 53 wafers submitted, only 28 were finally available for electrical testing. The processing yields of each run are shown in Table 14. The detailed run folders of each run were searched to find at which process steps the wafers were spoiled (except for run 1, for which the run folder has been lost). As shown in Table 15, most of the wafers spoiled in processing were lost during high-temperature steps. The cause of spoilage was cracking of the wafer in all cases except the photoresist steps. It is well known that SOS wafers are sensitive to thermal shock. Special instructions were included in the run sheets, specifying slow insertion and withdrawal from furnaces, for example, to protect the SOS wafers from such shocks. Nevertheless, wafers were cracked even in hot liquid etches. Such high losses are not at all typical of the SOS production runs at ATL. The problem here may exist precisely because these wafer lots were not regular production runs, and some of the personnel handling the lots may not have been familiar with the special handling precautions

Table 14
Processing Yield Analysis

Run Number	Wafers Started	Wafers Tested	Wafers Spoiled
1	15	11	4*
2	12	6	6
3	13	6	7
4	13	6	7
Totals	53	29	24

*Not accounted for in Table 15

Table 15
Analysis of Wafers Spoiled in Processing in Runs 2-4

Step	Temperature	Number of Wafers Spoiled
Oxidation	900 - 1000	4
Silox	900 - 950	3
Nitridation	850	4
Poly Deposition	950?	1
Diffusion	900 - 950	2
Anneal	900	2
Hot Acid Etch	180	2
Photoresist		3
Total		20

required for SOS. This result indicates that processing yield continues to be a concern for SOS.

The wafers that were successfully fabricated were electrically characterized by automated testing. The fabrication process, electrical tests, and parameter evaluations are described in Section 5. The device test data were stored on a large, demountable disc and transported to Westinghouse R&D. The voluminous data files were then translated into condensed numeric files for processing. All of the data was stored as ASCII character files. A program was written to sequentially read the files and to identify the fields that contain the required information. The files as written contain a lot of redundant information, such as labels and input variable values that are the same for each device test. By selecting the required data fields and translating the ASCII characters into numeric data in the APL programming language, a substantial reduction in memory requirement was achieved. Even so, the total data set was so large that the APL workspace size had to be increased to the maximum allowed on our computer.

Each device was tested at several bias points. From the measurements, calculations were made of leakage current, threshold voltage, mobility, and transconductance, as discussed in Section 5. The test data files contain numeric values for the four parameters listed. Hand calculations of several cases showed that the parameters were correctly computed according to the methods given in Section 5. The computer data transfer selected these parameter values and compiled them into a 12 by 4 array, giving the four parameters for each of the 12 devices tested in a single chip. Every wafer contained 12 chips that were tested, so the array of data from a wafer had dimensions 12 by 12 by 4. The test data records also included chip summaries, which gave the mean values and standard deviations for the four parameters and the percentage of devices, within the acceptable limits for each parameter. Wafer summaries were also included in the data records, which report the mean and standard deviations and percentage yields based on the four parameters. Initially, the wafer summaries were used to

perform correlations with the wafer UVS haze numbers. However, it was noted that some of the parameter values for different wafers were equal to 10 decimal places. Evidently a bug in the computer code of the test and data acquisition system led to improper selection of the raw data for compiling the chip and wafer summaries. To correct this problem, new summaries were made based on the individual device test records. The new summaries did not show any coincidences of mean values, indicating that there is no direct duplication of device test data itself. Also, several wafers were retested in different test runs, with close but not identical test results. The same acceptance limits were applied to all of the parameters, and only devices that passed all acceptance tests were considered to be good devices. The limits for leakage current were 1 nA and 10 μ A. The lower limit screens devices that are defective to the point of being completely open circuited. The upper limit represents an approximate design limit for circuit functionality. Threshold voltage limits were set to 0.1 and 2.0 volts, both being estimates of acceptable limits for circuit function. The mobility limits were 20 and 900 $\text{cm}^2/\mu\text{s}$, the lower limit rejecting poor devices and the upper limit rejecting irregular I-V curves. Similarly, the transconductance limits were 0.0005 to 100 S (ohms^{-1}) to assure adequate device performance and screen out irregular characteristics. The yield was defined as the percentage of good devices among the total number of devices tested on the wafer.

The tabulation of all electrical test data is given in Table 16. The wafer number is given along with the fabrication run numbers, followed by the mean and standard deviation over all good wafers for the leakage current, threshold voltage, mobility, and transconductance. The yield, UVS haze number, and vendor haze number are given in the last three columns. For the wafers which had no good devices, the number of devices which passed the acceptance limit of each parameter are given instead of the mean and standard deviation of the parameter. For example, in wafer 303, 143 out of 144 devices passed the leakage current acceptance limits, but only one device passed any of the

Table 16
Summary of Electrical Test Results

Wafer Number	Run Number	Leakage Current Average (uA)	Standard Deviation	Threshold Voltage Average (V)	Standard Deviation	Carrier Mobility Average (cm ² /VS)	Standard Deviation	Transconductance Average (mS)	Standard Deviation	Yield (percent)	UVS Haze Number	Reflectance Haze Number
14	1	0.42	0.43	0.45	0.05	75	11	1.46	0.03	91	168	40
21	4	0.27	0.19	0.48	0.05	95	8	0.91	0.03	98	110	0
26	1	0.86	1.00	0.42	0.07	261	73	1.23	0.26	90	143	0
46	1	0.49	0.25	0.46	0.03	312	12	1.43	0.06	92	143	0
49	1	0.19	0.71	0.44	0.07	260	53	1.34	0.03	92	143	0
50	1	0.23	0.65	0.70	0.09	298	64	1.00	0.03	92	143	0
52	3	0.59	1.93	0.48	0.03	376	54	1.03	0.03	95	143	0
56	1	0.61	1.74	0.73	0.07	98	12	1.37	0.22	79	143	0
62	4	0.78	2.08	0.24	0.03	947	67	1.12	0.10	79	143	0
71	2	0.04	0.59	0.42	0.06	99	21	1.44	0.05	76	143	0
72	2	0.51	0.72	0.34	0.03	103	44	1.17	0.10	95	143	0
73	3	0.50	0.77	0.71	0.13	232	51	1.00	0.10	14	143	0
85	3	0.24	0.37	0.42	0.06	34	45	0.96	0.10	73	143	0
84	2	0.08	0.08	0.44	0.04	79	16	1.07	0.05	40	143	0
102	4	0.40	0.15	0.59	0.15	277	46	1.36	0.07	85	143	0
106	2	0.01	0.02	0.42	0.02	107	13	0.86	0.08	65	143	0
107	3	0.06	0.08	0.39	0.02	69	53	1.26	0.13	25	143	0
108	3	0.13	0.45	0.42	0.06	73	71	1.37	0.07	93	143	0
108	3	0.05	0.45	1.36	0.22	172	61	0.93	0.17	90	143	0
303	4	0.15	0.45	1.36	0.22	267	61	0.90	0.13	90	143	0
304	1	143	0.93	1.00	1.00	15	0	0.00	0.00	0	1906	0
306	1	143	0.93	1.00	1.00	15	0	0.00	0.00	0	1711	0
307	1	144	0.93	1.00	1.00	15	0	0.00	0.00	0	1945	0
307	1	144	0.93	1.00	1.00	15	0	0.00	0.00	0	1579	0
307	1	144	0.93	1.00	1.00	15	0	0.00	0.00	0	1377	0
406	4	0.01	0.01	0.76	0.08	72	7	0.87	0.02	96	364	0
415	1	2.60	2.07	0.49	0.07	422	35	1.35	0.06	45	348	0
415	1	0.08	0.23	0.53	0.05	275	102	1.37	0.16	44	348	0
421	1	1.33	0.05	0.53	0.05	1	1	1.37	0.05	0	1741	0

other acceptance tests. This indicates devices which are totally nonfunctional. The statistical tests described below are based on this data table.

6.2 Statistical Analysis of Test Data

The measurement data are analyzed next by using scatter plots and correlation coefficients. The yield of devices per wafer is shown plotted against the UVS haze number in the scatter plot shown in Figure 69, with data for all SOS wafers tested. The haze number is shown on a logarithmic scale to accommodate the wide range of variation. No clear trend is evident in the inclusive data set.

The analysis is placed on a quantitative basis by tabulation of the correlations of device yield and parameters with haze. The correlation coefficient measures the amount of the linear variation in a dependent variable (yield, threshold, etc.) that can be attributed to variation in an independent variable (haze). If the correlation is +1 (or -1), then the dependent variable can be computed exactly, in the given data set, as a linearly increasing (or decreasing) function of the dependent variable. The correlations are tabulated in Table 17. The first entry in the table defines the group for which the correlation was taken. The entries include all SOS wafers taken together, all wafers with non-zero yield, all vendor wafers, and each of these categories by run number. For each group, the number of data points and the number of remeasurements in the data set are given. Both UVS haze and the UV reflectance haze provided by the vendor have been analyzed. The UV reflectance correlations can only be taken on groups of vendor wafers, since reflectance data is not available for Westinghouse wafers. Correlation of yield is given for each group, but the correlation of the device parameters is only given for groups of non-zero yield wafers, since there are no data on device parameters for the bad wafers. The correlation coefficients are taken between the yield (or other parameter) and the linear haze number. Correlations were also run with the logarithm of the UVS haze number for comparison. The magnitude of

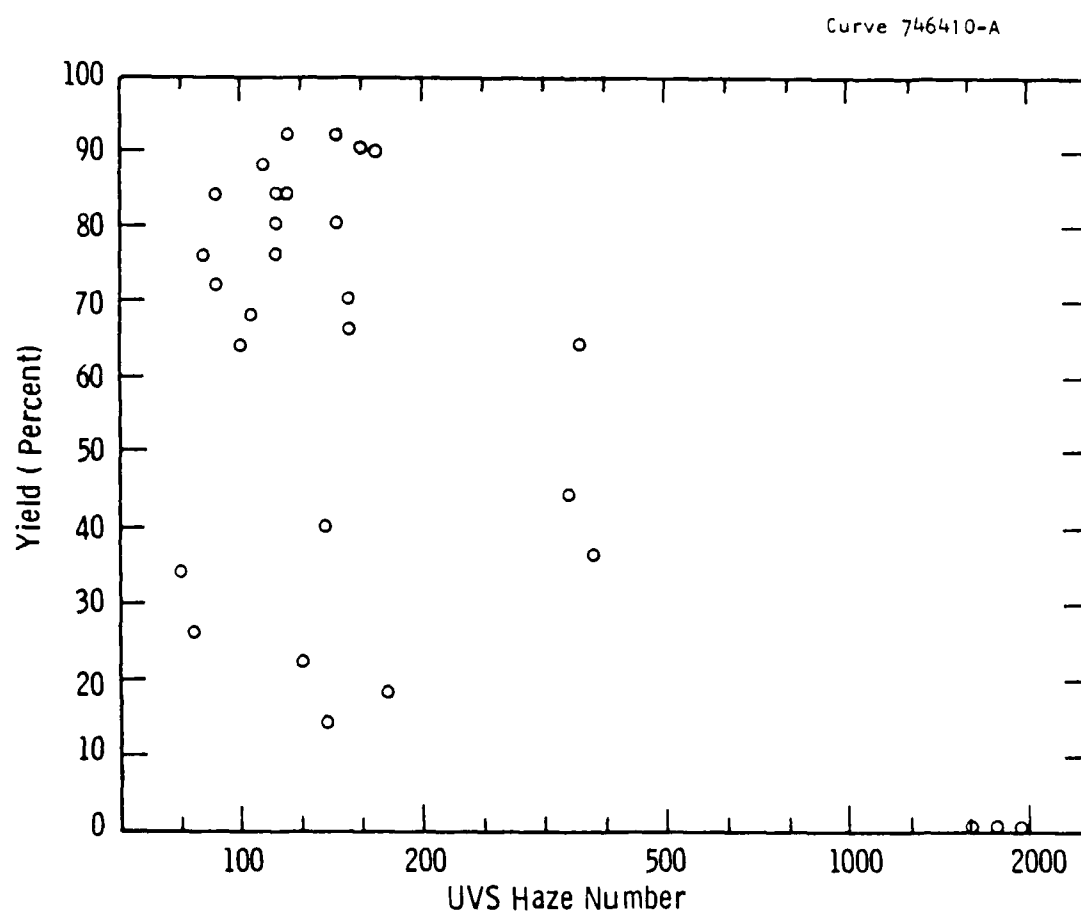


Figure 69. Device yield results for all SOS wafers fabricated.

Linear Correlations with Haze Number

	Number of Points	Number of Repeats	Type of Haze	Yield	Leakage Current	Threshold Voltage	Carrier Mobility	Transconductance
All SOS	33	4	UVS	-.72				
Good SOS	27	3	UVS	-.19	.07	-.02	.22	.10
Vendor	24	3	UVS	-.05	.27	-.10	.23	.02
Run 1: All SOS	11	0	REF	.46	-.12	.57	-.05	-.24
Good SOS	8	0	UVS	-.86				
Vendor	6	0	UVS	-.25	-.31	-.64	.28	.11
Run 2: Vendor	6	0	REF	.75	-.76	.05	-.59	-.05
	6	0	REF	.37	-.32	.41	-.88	.41
Run 3: All SOS	10	4	UVS	-.03	-.02	-.23	.21	.26
Vendor	8	3	UVS	0	0	0	0	0
Run 4: All SOS	8	3	UVS	-.64				
Vendor	8	3	REF	-.65	.66	-.64	.56	.88
	8	3	REF	.88	-.32	.81	-.52	-.53
Run 4: All SOS	6	0	UVS	-.90				
All Good SOS	5	0	UVS	-.85	-.75	.77	-.94	-.85
Vendor	4	0	UVS	.47	.71	.73	-.24	-.06
	4	0	REF	.56	-.84	-.25	-.04	-.84

the correlation was within + 0.5 to -.11 of the corresponding linear haze correlation. It is considered that the linear haze correlations adequately represent the behavior of the parameters with respect to haze.

The data plotted in Figure 69 correspond to the first entry in Table 17. The -.72 correlation indicates a tendency for yield to decrease at higher haze numbers. This is largely due to the zero yields obtained on the low-temperature epi wafers. When the zero-yield wafers are deleted, the remaining data are described by a smaller correlation, shown in line 2 of Table 17. The data are shown in Figure 70. Over the relatively limited range of haze numbers observed among the vendor wafers, there is no discernable trend. The same yield data are plotted against the UV reflectivity haze data provided by the vendor in Figure 71. Here it can be seen that there is an apparent positive trend, due to the high yields of some wafers with haze numbers of 5 or 6, and the low yields of some wafers with zero haze numbers. This is reflected quantitatively in the .46 correlation coefficient for this group of wafers, shown in Table 17.

Next, the data are presented and analyzed on a run-by-run basis. This will discriminate against factors such as processing variations that affect the yield and performance of individual runs. Figure 72 shows the yield data for Run 1. Three low-temperature epi wafers, W304, 306, and 421, in this run showed zero yield of good devices. This is consistent with the zero yield observed in low-temperature epi wafers W301 and 307 in other runs. (Note that in the second oral presentation and viewgraphs, wafer 421 was incorrectly identified. The confusion arose between wafers W40 and W421, which were intended to be wafer numbers 5 and 15, respectively, in Run 1. The wafers were incorrectly labelled by etching the epilayer. The incorrect labels were changed by scribing new numbers over the etched numbers, before sending the wafers to ATL, that were not properly read by the operator when the run sequence numbers were inscribed by photolithography at ATL.) As a result of the zero yield for the high-haze wafers, the correlation is

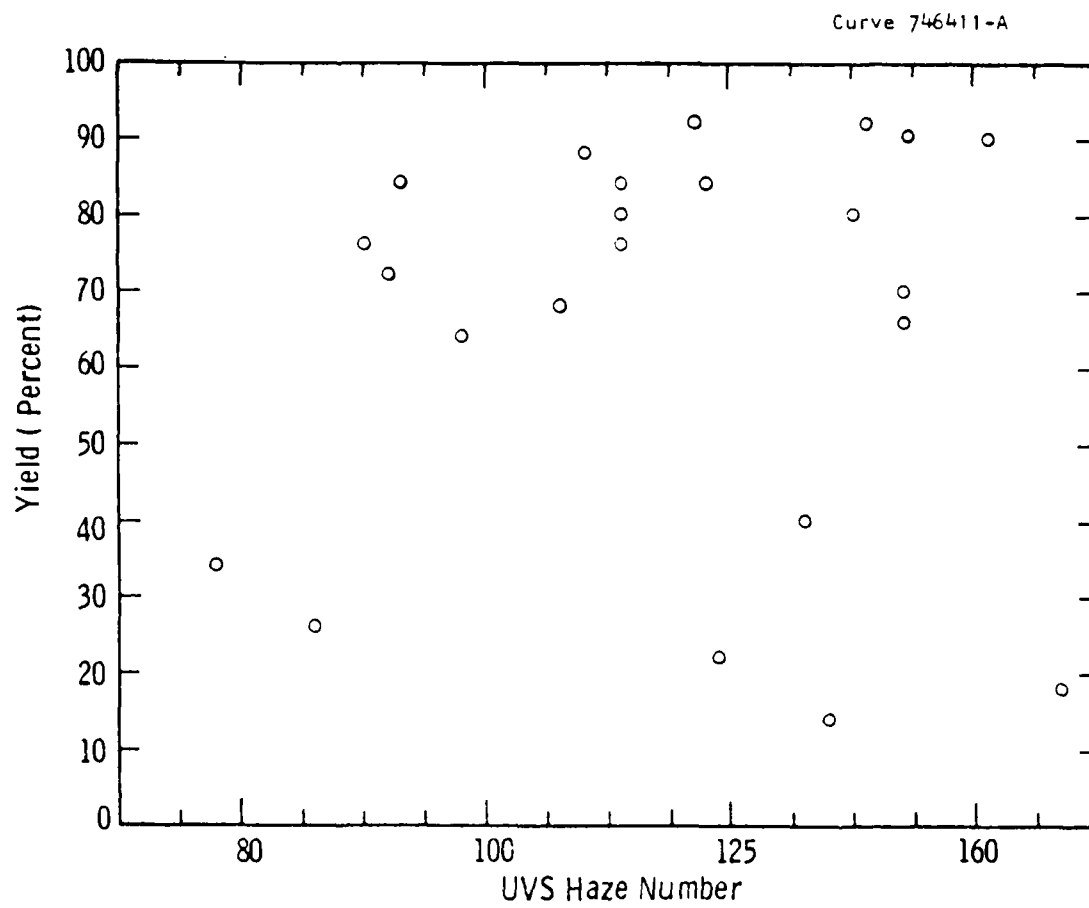


Figure 70. Device yields for vendor wafers.

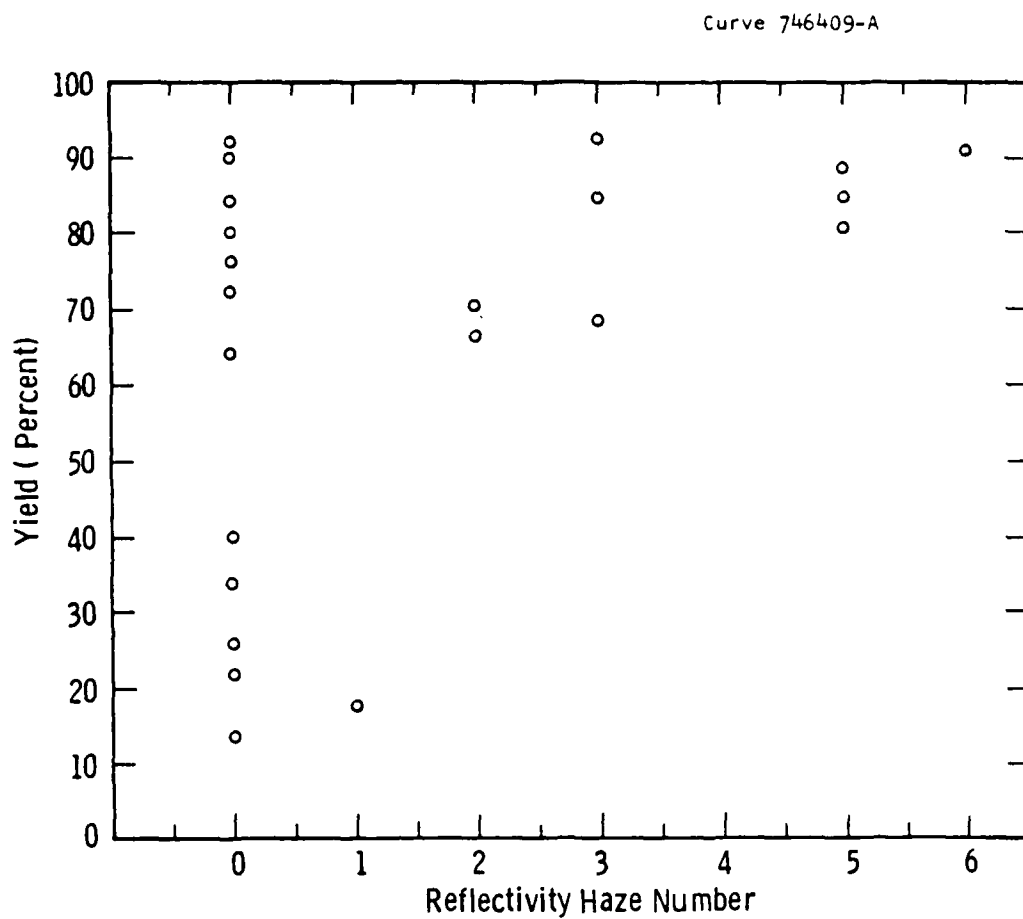


Figure 71. Device yields for all vendor wafers, plotted against vendor-supplied UV reflectivity haze data.

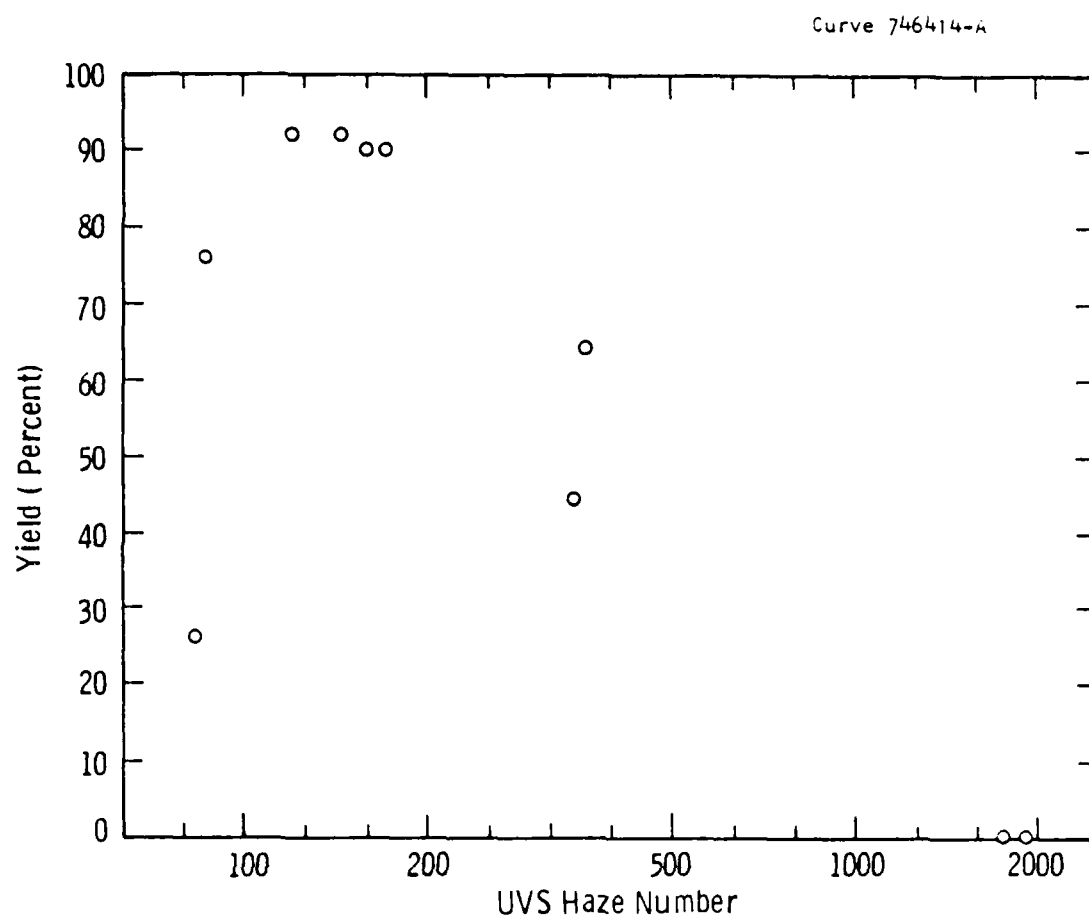


Figure 72. Device yields for Run 1.

strongly negative at $-.86$. When only the good wafers with non-zero yield are considered, the correlation drops to $-.25$, which shows the influence of the two Westinghouse wafers of moderate yield and haze numbers near 400. Finally, when only the vendor wafers are considered, both the UVS and reflectance haze give positive correlations of $.75$ and $.37$, respectively.

The data for Run 2 are presented in Figure 73. In this run, only vendor wafers with non-zero yield appear. The UVS haze correlation is very low at $-.03$. No correlation can be made with reflectance haze because all six wafers from this run had zero haze numbers by the reflectance method. Figure 74 shows the yield data for Run 3. There is a definite downward trend in yield with UVS haze, with correlations of $-.64$ for the entire group and $-.65$ for the vendor wafers. The reflectance haze gives a positive correlation of $.88$. The data for Run 4 are shown in Figure 75. The UVS haze shows a negative correlation of $-.90$ for the entire group including the zero-yield low-temperature epilayer, and $-.85$ when only good wafers are included. However, for the vendor wafers the UVS haze gives a positive $.47$ correlation, and the reflectance haze again gives positive correlation at $.56$.

The statistical significances of the correlations can be determined by a t-test. The expression

$$S = r \left(\frac{n-2}{1-r^2} \right)^{1/2}$$

gives a parameter S for a data set with correlation coefficient r and number of sample points n .⁽³¹⁾ The parameter S is compared to a t-test with $n-2$ degrees of freedom to determine significance. In Table 18 the yield correlations are summarized. A single asterisk by an entry in the table denotes statistical significance at the 0.1 level, and two asterisks denotes significance at the 0.01 level. The UVS haze correlations are all negative and statistically significant for the groups that contain high haze wafers which had zero yield. However,

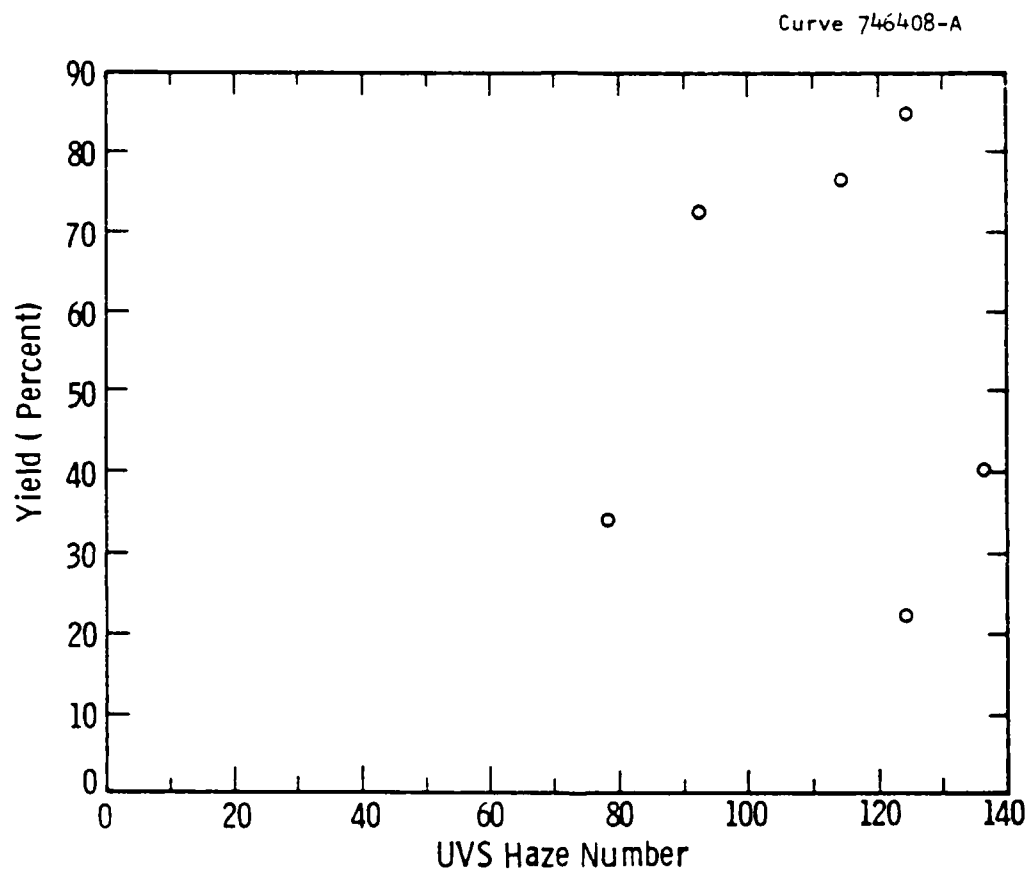


Figure 73. Device yields for Run 2.

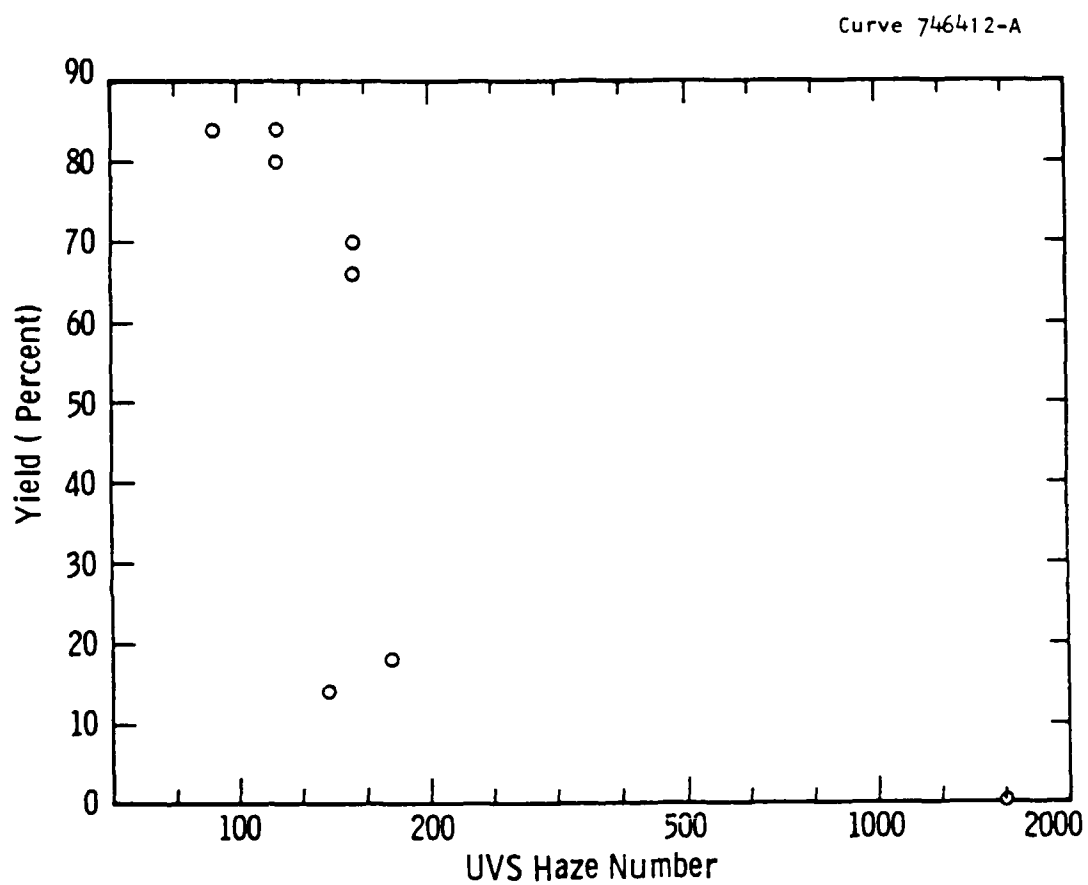


Figure 74. Device yields for Run 3.

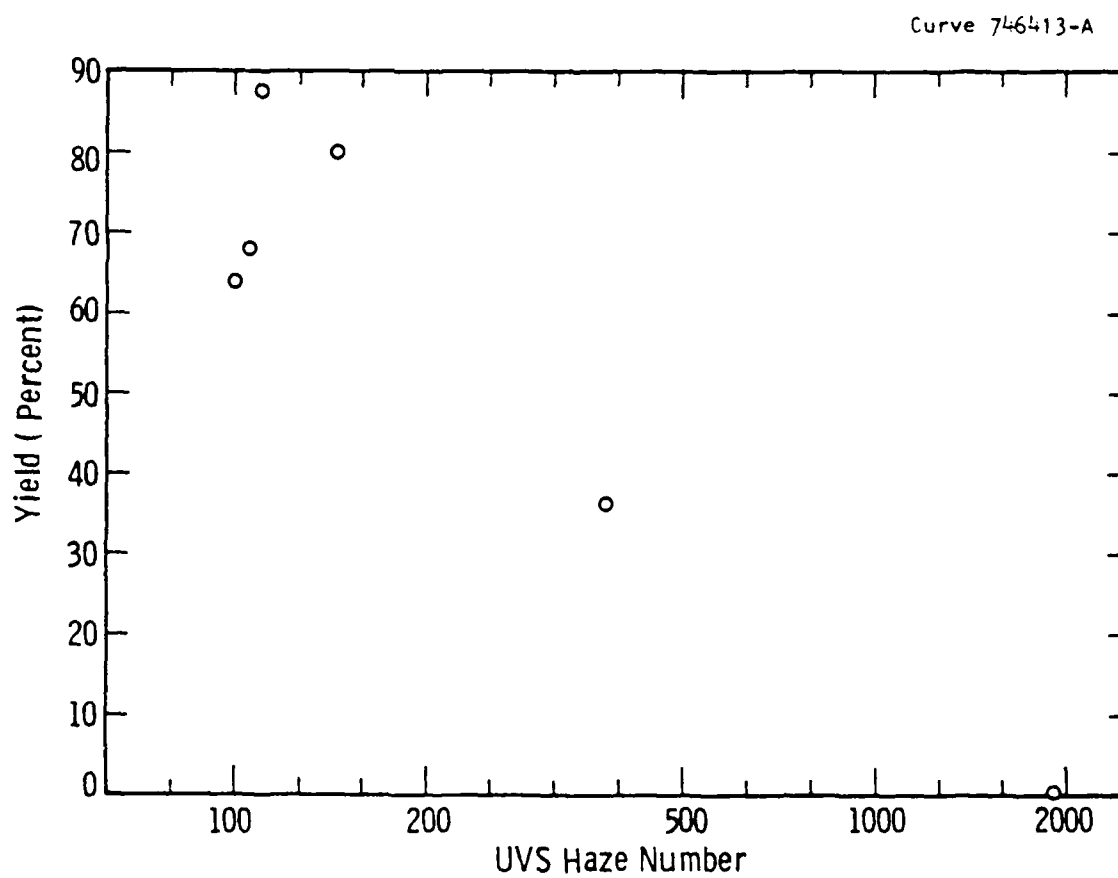


Figure 75. Device yields for Run 4.

when the data set is restricted to wafers with non-zero yield, or to vendor wafers, fewer of the correlations are significant. Two of the significant correlations are negative and one is positive. For this reason we conclude that the UVS haze is not a reliable predictor of eventual device yield, except for wafers with very high haze numbers. The reflectance haze correlations are all positive and three are statistically significant. Although contrary to expectation, this would indicate that low-reflectance haze numbers are associated with low yields.

The correlations for device parameters are also shown in Table 17. Among the large groups of good SOS wafers and vendor wafers, only one correlation is statistically significant at the 0.01 level; that is, the correlation of threshold voltage with reflectance haze. In individual runs, there are high correlations, but from one run to the next the sign of the correlation is likely to change. There is no consistent correlation between device parameters and haze.

Correlations were also performed between wafer yield and wafer bow, flatness, epilayer thickness, and Raman shift. The correlation coefficients were not statistically significant.

Table 18
Statistical Significance of Yield Correlations

	UVS Haze		Reflectance Haze	
	All Wafers	Good Wafers	Vendor Wafers	Vendor Wafers
All runs	-.72**	-.19	-.05	.46**
Run 1	-.86*	-.25	.75*	.37*
Run 2			-.03	0
Run 3	-.64*		-.65*	.88**
Run 4	-.90**	-.85*	.47	.56

* Significant at .1 level

**Significant at .01 level

7. DISCUSSION OF RESULTS AND CONCLUSIONS

In the course of this program, SOS wafers from several sources were characterized by structural properties; devices were fabricated and tested, and correlations were sought between the initial tests and final device performance. In this section, an overview of the results is presented, with the conclusions concerning the quality of the SOS material, applicability of characterization methods, and their relation to device yield and performance.

The vendor wafers were checked for compliance with the purchase order specifications by optical inspection and measurement. Wafer bow and flatness were measured interferometrically with a Tropel wafer flatness analyzer. Epilayer thickness was measured at five points on each wafer by reflectance interference versus wavelength. The substrate orientation was verified on selected wafers by X-ray. All of the vendor wafers met the specifications in terms of visible flaws such as scratches, pinholes, orange peel, cracks, and chips. The specifications for bow and flatness were also satisfied. The epilayer thickness specification was a 500 nm target thickness with a $\pm 10\%$ tolerance. For two wafers the average thickness was slightly below the tolerance limits of 450 nm. However, the local thickness was out of specification more often. A total of nine measurement points were too thin, and 30 measurement points were too thick. This reflects a problem with thickness uniformity on a single wafer. Epilayer thickness measurements were taken at the center of each wafer and at four points halfway between center and edge. All of these points are within the nominal central region of the wafer, where the material quality must be high for good chip yield. Of the vendor wafers, 37 wafers have a 10% or greater variation in epilayer thickness over this area, with a maximum observed of 17%.

Recent measurements on 4-inch SOS wafers show a significant difference between vendors with regard to epilayer uniformity. Nineteen wafers from Kyocera were measured at five points. The total range of epilayer thickness was $\pm 5\%$ from the mean. The maximum variation of 7% on a single wafer is substantially lower, on a 4-inch wafer, than our previous result of 17% on a 2-inch wafer. A single Union Carbide 4-inch wafer was measured at five points and showed an 11% range of variation in epi thickness.

These observations lead us to the conclusion that among the ordinary wafer specifications, only the epilayer thickness and thickness uniformity are problem areas.

The Raman shift measurements of epilayer stress did not reveal a significant variation of stress among the vendor wafers. The Westinghouse wafers with epilayers grown at normal temperatures also showed the same stress level as the vendor wafers. Only the low-temperature epilayers showed a lower stress, but at the same time showed an increased linewidth indicative of poor crystal quality. Two SOS wafers with solid-phase regrown epilayers also showed reduced stress. The applicability of this measurement is limited by the repeatability of measurements on a silicon crystal wafer. The instrument resolution was set at a level which allowed the rapid determination of Raman shift in a manner that would be suitable for 100% screening of wafers. Remeasurements of a silicon wafer under these conditions showed the same range of variation as the SOS wafers. Increased resolution can be achieved with the same instrumentation, but the time required to examine a single wafer becomes comparable to X-ray techniques. Correlation of the Raman shifts with device yields and performance shows no statistically significant relationship. Our conclusion is that there is little variation in epilayer stress among wafers subjected to the same growth temperature and standard CVD deposition. The epilayer stress cannot serve as a significant screening factor.

The haze measurement technique based on UV scattering has been shown to be a more precise measurement than the UV reflectance method. For each wafer a definite, non-zero haze reading is obtained that is repeatable in successive measurements and stable when repeated after a long time interval. The haze has been shown to depend on the rotation angle of view between the detector and the c-axis of the sapphire substrate. This angular dependence, and the haze as measured at a fixed orientation angle, were shown to originate in the surface texture of the silicon epilayer. Other methods of observing the surface texture, including TEM surface replicas, cross-section TEM views, Nomarski optical microscopy, and profilometry, were inconclusive in adding information about the nature of the surface texture. The distinguishing feature of the angular dependence of scattering, first discovered in the course of this program, is the presence of either two or four scattering peaks symmetrically disposed with respect to the c-axis projection on the sapphire substrate. Such peaks are observed in Union Carbide 2- and 4-inch wafers, epilayers grown at normal temperatures at Westinghouse, and in Kyocera 4-inch wafers. There is a considerable range of variation in the height of the peaks and in the relative amplitudes of the two major and two minor peaks. The significance of these variations has not been determined. Our tentative conclusion concerning UV scattering is that this is a very sensitive tool for observing the surface texture of the silicon epilayer, but more intensive study is required before the results can be properly interpreted in terms of the details of the crystal structure of the epilayer.

The haze measured by UV scattering is related to the crystal quality in the epilayer, at least in a qualitative way. The low-temperature epilayers, grown to provide an example of poor-quality material, show a haze level that is 20 to 30 times higher than the vendor wafers. The Westinghouse high-temperature epilayers also show higher haze ranging about 4 to 6 times as high as the vendor wafers. Within the set of vendor wafers, the haze readings vary by about a factor of 2. Recently examined Union Carbide 4-inch wafers have the

same range of haze as the 2-inch wafers studied in this program. Recently examined Kyocera 4-inch wafers have very low haze, about 30 to 50% as high as the Union Carbide 2-inch wafers. Our conclusion is that a certain range of variation can be expected for wafers from different epi reactors. This is consistent with the different calibrations required for UV reflectance haze for wafers from different reactors.⁽²⁶⁾ Wafers can be of good quality if the measured haze lies within the range that is characteristic of the type of epi reactor. Wafers with extraordinarily high haze can be identified as defective. This is further clarified by the electrical test results described below.

SOS wafers were processed at Westinghouse ATL to fabricate p- and n-channel MOSFETs. Many wafers were spoiled in processing. The major cause of difficulty was cracking of the wafers in high-temperature processing steps. This occurred despite instructions for slow heating and cooling to avoid thermal shock. Our conclusion is that losses during processing due to breakage are still a yield factor to be considered. A minor case of difficulty was spoilage by improper photolithography. The wafers that emerged from processing were electrically tested to determine the yield of devices that passed acceptable limits on leakage current, threshold voltage, mobility, and transconductance. The observed yield and the measured parameters were then correlated with the previously measured UV scattering haze, the UV reflectance haze measured by the vendor, and other characterization parameters. The principal result is that the very high haze, low-temperature epi, SOS wafers had very low device yields. However, among the vendor wafers, and among the Westinghouse epilayers grown at normal temperatures, there was no significant correlation between haze and device yield or other performance parameters. This result is the same when the wafers are treated as a single group, and when the data are examined run by run to discriminate against process-induced variations. Our conclusion is that the vendor wafers, and the Westinghouse normal temperature epilayers, were good enough so that the starting material quality was not a limiting factor in determining yield.

Correlations were also run between device yield and parameters, and characterization data including wafer flatness, wafer bow, epilayer thickness, and Raman shift data on layer stress. No statistically significant correlations were observed.

8. REFERENCES

1. W. E. Ham, "The Electrical Characterization of Heteroepitaxial Semiconducting Films," in *Heteroepitaxial Semiconductors for Electronic Devices*, ed. G. W. Cullen, C. C. Wang (Springer-Verlag, 1978).
2. D. E. Passoja, D. McLeod, L. G. Dowell, H. F. Hillery, J. E. A. Maurits, and L. R. Rothrock, "Some Aspects of the Structure-Properties Relationships Associated with Haze in SOS," *J. Crystal Growth*, Vol. 58, pp. 44-52 (1982).
3. J. Lagowski, L. Jastrzebski, and G. W. Cullen, "Electronic Characterization of Heteroepitaxial SOS by Surface Photovoltage Spectroscopy," *J. El. Chem. Soc.* Vol. 128, pp. 2665-2670 (1981).
4. M. S. Abrahams and C. J. Buicocchi, "Cross-Sectional Electron Microscopy of Silicon on Sapphire," *Appl. Phys. Lett.* 27, pp. 325-327 (1975).
5. R. Lihl, H. Oppolzer, P. Pongratz, P. Skalicky, and W. Svanda, "Electron Microscope Study of Microtwins in Epitaxial Silicon Films on Sapphire," *Journal of Microscopy*, Vol. 118, Pt. 1, pp. 89-95 (1980).
6. F. A. Ponce and J. Aranovich, "Imaging of the Silicon on Sapphire Interface by High Resolution TEM," *Appl. Phys. Lett.* 38, pp. 439-441 (1981).
7. J. H. Chang, "Channeling Analysis of Defect Distribution in Epitaxial Si Layers," *Nuclear Instruments and Methods*, Vol. 173, pp. 565-570 (1980).
8. A. Gupta and P. K. Vasudev, "Recent Advances in Heteroepitaxial Silicon on Insulator Technology," *Solid State Technology*, pp. 104-109 (Feb. 1983).
9. A. Rey, J. Trilhe, and J. Borel, "The Application of Automatic X-Ray Rocking Curves to the Characterization of Silicon on Sapphire," *J. Crystal Growth* 60, pp. 264-274 (1982).
10. R. T. Smith and C. E. Weitzel, "Influence of Sapphire Substrate Orientation on SOS Crystalline Quality and SOS/MOS Transistor Mobility," *J. Cryst. Growth*, Vol. 58, pp. 61-72 (1982).

11. T. Yoshii, S. Taguchi, T. Inoue, and H. Tango, "Improvement of SOS Device Performance by Solid Phase Epitaxy," Proc. 13th Conf. on Solid State Devices, Toyko, 1981; Jpn. J. Appl. Phys., Vol 21, Suppl. 21-1, pp. 175-179 (1982).
12. A. Gupta and P. K. Vasudev, "Recent Advances in Heteroepitaxial Silicon on Insulator Technology," Solid State Tech., pp. 129-134 (June 1983).
13. M. T. Duffy, J. F. Corboy, G. W. Cullen, R. T. Smith, R. A. Soltis, G. Harbeke, J. R. Sandercock, and M. Blumenfeld, "Measurement of the Near-Surface Crystallinity of Silicon on Sapphire by UV Reflectance," J. Cryst. Gr., Vol. 58, pp. 10-18 (1982).
14. T. Englert, G. Abstreiter, and J. Pontcharra, "Determination of Existing Stress in Silicon Films on Sapphire Substrate Using Raman Spectroscopy," Solid State Electron. 23, 31 (1980).
15. J. F. Hall, W. F. C. Ferguson, "Optical Properties of CdS and ZnS from 0.6 to 14 microns," J. Opt. Soc. Am. Vol. 45, pp. 714-718 (1955).
16. H. W. Verleur, "Determination of Optical Constants from Reflectance or Transmittance Measurements on Bulk Crystals or Thin Films," J. Opt. Soc. Am. Vol. 58, pp. 1356-1364 (1968).
17. T. Huen, "Reflectance of Thinly Oxidized Silicon at Normal Incidence," Appl. Opt. Vol. 18, pp. 1927-1932 (1979).
18. Y. Nishi and H. Hara, "Physics and Device Technology of Silicon on Sapphire," Proc. 9th Conf. on Solid State Devices, Tokyo, 1977; Jpn. J. Appl. Phys. Vol. 17, Suppl. 17-1, pp. 27-35 (1978).
19. G. A. Sai-Halasz, F. F. Fang, T. O. Sedgwick, and Armin Segmuller, "Stress-Relieved Regrowth of Silicon on Sapphire by Laser Annealing," Appl. Phys. Lett. 36, 419 (1980).
20. J. Hyncek, "Elastoresistance of n-type Silicon on Sapphire," J. Appl. Phys. 45, 2631-2635 (1974).
21. A. J. Hughes, "Stress-Induced Anisotropy in the Electrical Properties of SOS," J. Appl. Phys. Vol. 46, p. 2849-2863 (1975).
22. E. Anastassakis, A. Pinczuk, and E. Burstein, "Effect of Static Uniaxial Stress on the Raman Spectrum of Silicon," Solid State Commun. 3, 133 (1979).
23. K. Yamazaki, M. Yamada, K. Yamamoto, and K. Abe, "Relief of Residual Strain in Silicon on Sapphire by Heat-Assisted Pulsed Laser Annealing," Jpn. J. Appl. Phys. 20, 1299 (1981).

24. J. M. Elson and J. M. Bennett, "Relation Between the Angular Dependence of Scattering and the Statistical Properties of Optical Surfaces," J. Opt. Soc. Am. 69, pp. 31-47 (1979).
25. G. W. Cullen, M. S. Abrahams, J. F. Corboy, M. T. Duffy, W. E. Ham, L. Jastrzebski, R. T. Smith, M. Blumenfeld, G. Harbeke, and J. Lagowski, "Characterization of Heteroepitaxial Silicon," J. Crystal Growth, Vol. 56, pp. 281-295 (1982).
26. M. T. Duffy, P. J. Zanzucchi, W. E. Ham, J. F. Corboy, G. W. Cullen, and R. T. Smith, "Optical Characterization of Silicon and Sapphire Surfaces as Related to SOS Discrete Device Performance," J. Cryst. Gr. Vol. 58, pp. 19-36 (1982).
27. P. J. Zanzucchi and M. T. Duffy, "Surface Damage and the Optical Reflectance of Single Crystal Silicon," Appl. Opt. 17, pp. 3477-3481 (1978).
28. D. E. Aspnes and A. A. Studna, "Dielectric Functions and Optical Parameters of Si, Ge, GaP, GaAs, GaSb, InP, InAs, and InSb from 1.5 to 6.0 eV," Phys. Rev. B. Vol. 27, pp. 985-1009 (1983).
29. D. V. Lang, "Deep-Level Transient Spectroscopy: A New Method to Characterize Traps in Semiconductors," J. Appl. Phys., 45, 3023 (1974).
30. J. W. Chen, R. J. Ko, D. W. Brzezinski, L. Forbes and C. J. Dell'oca, "Bulk Traps in Silicon-on-Sapphire by Conductance DLTS," IEEE Trans. Electron Devices, ED-28, 299 (1981).
31. G. A. Korn and T. M. Korn, Mathematical Handbook for Scientists and Engineers, McGraw-Hill (1968), p. 700.

ACKNOWLEDGEMENTS

It is a pleasure to acknowledge the technical contributions made by co-workers during the progress of this work. W. Choyke provided the Rutherford backscattering measurements. J. Gregg did the cross sectional transmission electron microscope work. S. Dutta assisted in the Raman measurements and D. Meier performed the CDLTS measurements. M. Hanes advised us on the growth of epilayers. C. Scott directed the device fabrication and testing at Baltimore ATL. P. Rai-Choudhury also advised us on epilayer growth, and provided the managerial direction.

It is also a pleasure to acknowledge the capable technical assistance of R. Hauser, for measurements of haze, flatness bow, and thickness, W. Cifone for epilayer growth, and F. S. Youngk and G. J. Machiko for design and assembly of measurement apparatus.



*MISSION
of
Rome Air Development Center*

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C³I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

END

FILMED

3-85

DTIC